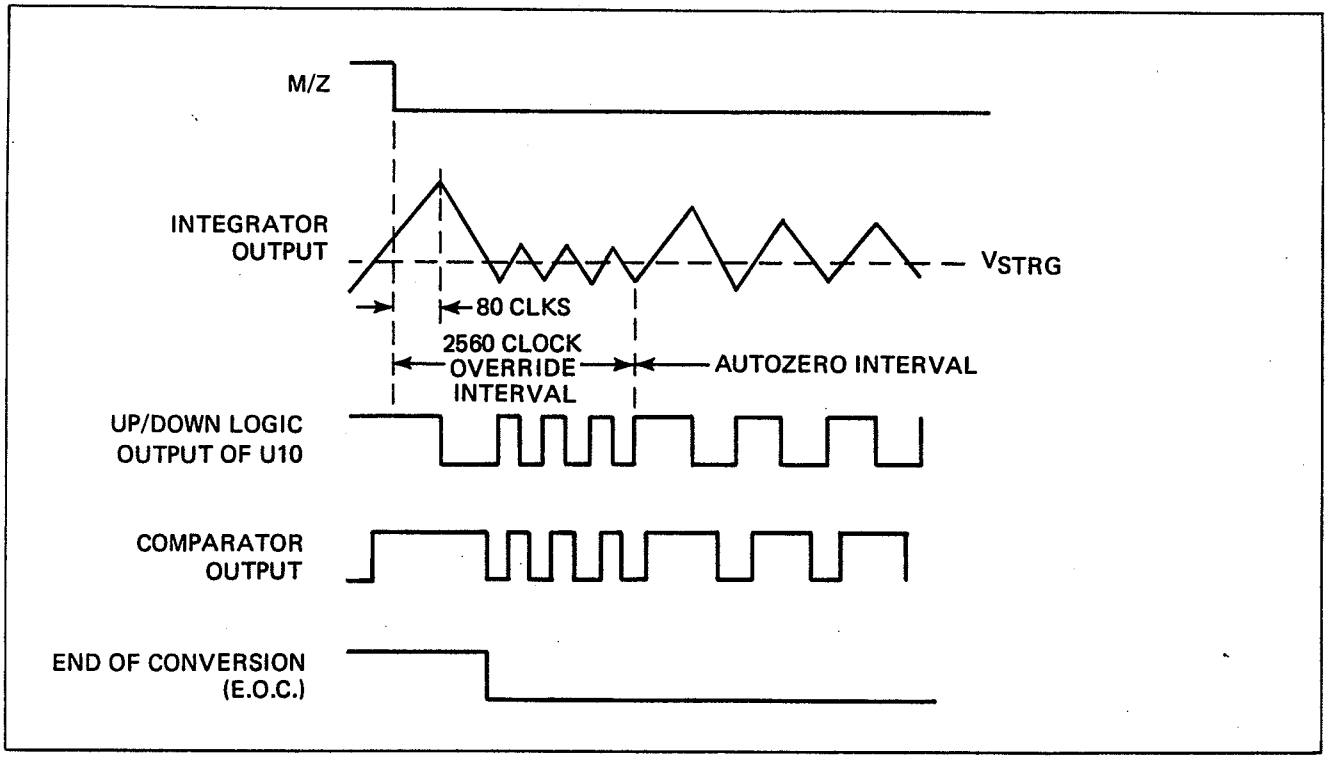


Figure 4.12A - Waveforms During Override Interval (Integrator Output More Positive Than V_{strg} At End of Measure Interval).

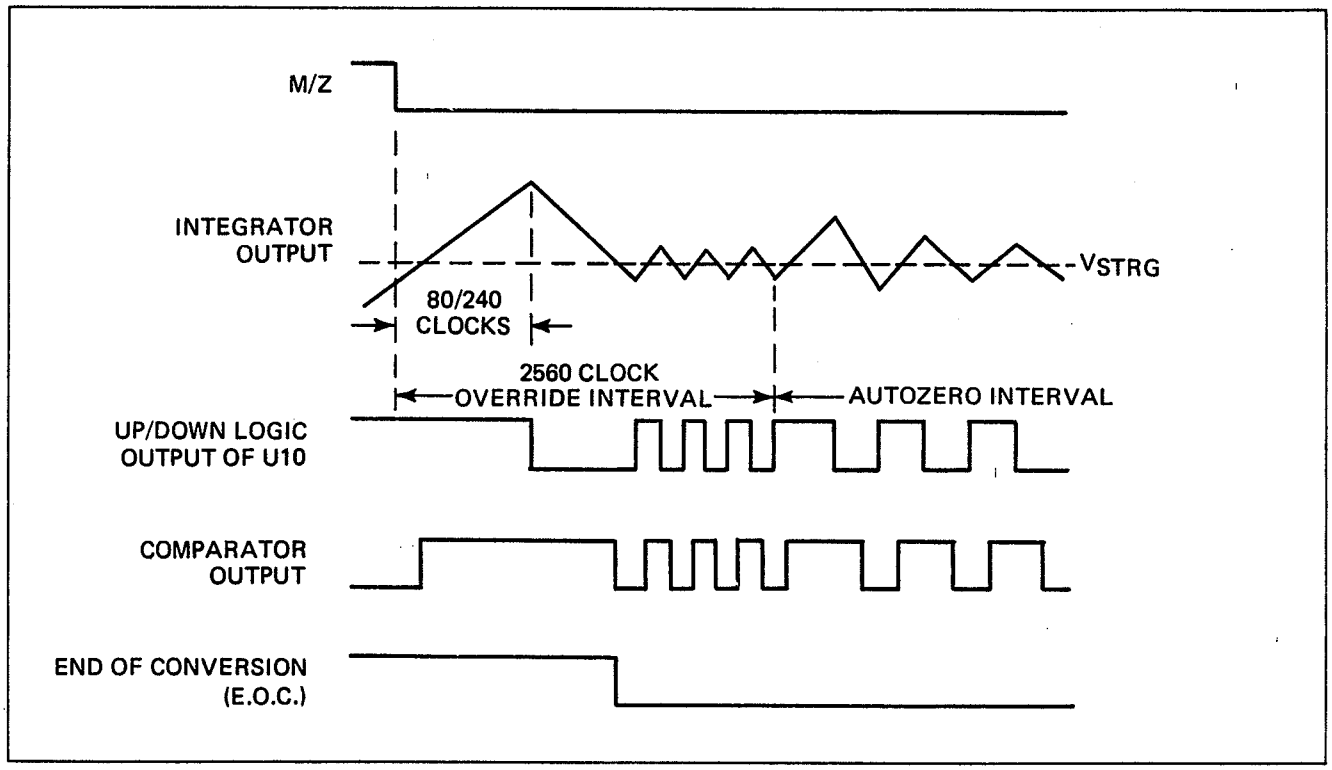


Figure 4.12B - Waveforms During Override Interval (Integrator Output More Negative Than V_{strg} At End of Measure Interval)

an interval at the beginning of Auto-Zero called the "Override Interval". The Override Interval is a fixed 2560 counts long (1.04 ms in a 60 Hz instrument). During the Override Interval the input of AR5 (Input Buffer) is switched to ground through M/Z switch U26, but the AZ Filter remains disconnected from the Integrator output (Q9 is OFF). When the Measure Interval ends, the Integrator output will be either higher or lower than Vstrg. Override Interval waveforms for both conditions are shown in Figure 4.12A and B.

4.4.6 Digitizer Counter & Control Output.

4.4.6.1 The 4 bit BCD data stored in the data latches of U10 are multiplexed and routed through the opto-isolator drivers U9 and U17, and presented one digit at a time to the microprocessor control section of the DMM.

4.4.6.2 The A/D output control signals are:

a) END OF CONVERSION: Advises μP that A/D conversion is completed and that a reading is ready.

b) 1 KHz: Synchronizes data transfer between A/D and μP.

c) DIGIT STROBE SYNC D6: Advises μP when the sixth BCD digit is being transmitted.

d) POLARITY: Polarity information passed on to the μP (+ or – input).

4.5 DIGITAL THEORY OF OPERATION.

4.5.1 Digital Hardware Description.

4.5.1.1 The DMM's digital control centers around U35, (Dwg. on page 6-10), a 6802 microprocessor which executes the program contained in ROMs, reads data from various locations throughout the DMM and stores data to RAM and to various hardware locations throughout the DMM. The microprocessor executes the ROM program based on these data, performs calculations, and makes decisions to control all the functions described in Section 3 of this manual.

4.5.1.2 The hardware locations contributing data to the microprocessor are the Digitizer (via opto-couplers OCI1 and OCI2), the keyboard on the front panel, and through the GPIA (U44) which passes commands from the 488 bus to the μP. This group is located at Sections 6, 7, 8 and 9 as shown in Figure 4.1.

4.5.1.3 In turn, the microprocessor outputs processed data to the GPIA and LED display. The μP also sends control information to the Digitizer and the analog hardware via opto-isolator OCI3. The Figure 4.13 graphically presents the hardware network controlled by the microprocessor. The schematic drawing on page 6-11 listed in Section 6 presents the coded designators that input and output to/from the microprocessor through the opto couplers.

4.5.2 The Microprocessor Section.

4.5.2.1 The microprocessor section (MPU) located in Section 6 on the motherboard consists of the microprocessor U35, with program memory IC's U27, U28, U29 and U30, address decoders U14 and U15, interrupt control hardware U2, U6 and U20, and non-volatile memory system U43, U42, VR12, BT1 and Q21. The complete schematic drawing is listed in section six pages 6-10 and 6-13.

4.5.2.2 When power is first applied to the microprocessor (μP), the R76-C75 time constant on the μP's RESET input (U35-40) holds the μP in reset long enough for the power supplies and clock to stabilize, then reset goes high (HI) enabling the start-up routine.

4.5.2.3 The DMM system clock is generated by the μP combining internal components with external components connected to pin U35-38 and U35-39 comprising of a 3.579 MHz crystal Y1 and C73-C76 components. The μP divides this frequency by four then outputs at pins U35-37 as 'E' the system clock of 895 KHz (approx.) for all μP bus components.

4.5.3 Program Memory.

4.5.3.1 The entire program memory for the μP resides in ROM's U27 through U30. IC's U27, U29, U28 and U30 are connected so that each can hold a 2Kx8 model 2716 EPROM or U29 and U30 can be omitted and U27 and U28 can each contain a 4Kx8 ROM. The μP directs other hardware locations dedicated to specific memory assignments as the Non-Volatile-Memory; GPIA and Digitizer.

4.5.4 Address Decoding.

4.5.4.1 The IC's U14 and U15 comprise the address decoding hardware used by the μP. The inputs to the address decoders are various address lines from the μP as well as other control lines. Each decoder has 8 normally high outputs, AY0 to AY7 and BY0 to BY7 which are used as 'Chip selects' for various hardware throughout the DMM. When the μP places an address on its address bus, U14 and/or U15 decode this address and supply the required chip select to the selected component which is being addressed by the μP.

4.5.4.2 The outputs of U14 are not gated internally with the clock, therefore the negative pulse widths may vary from 900 to 1200 ns. The outputs from U15 are internally gated

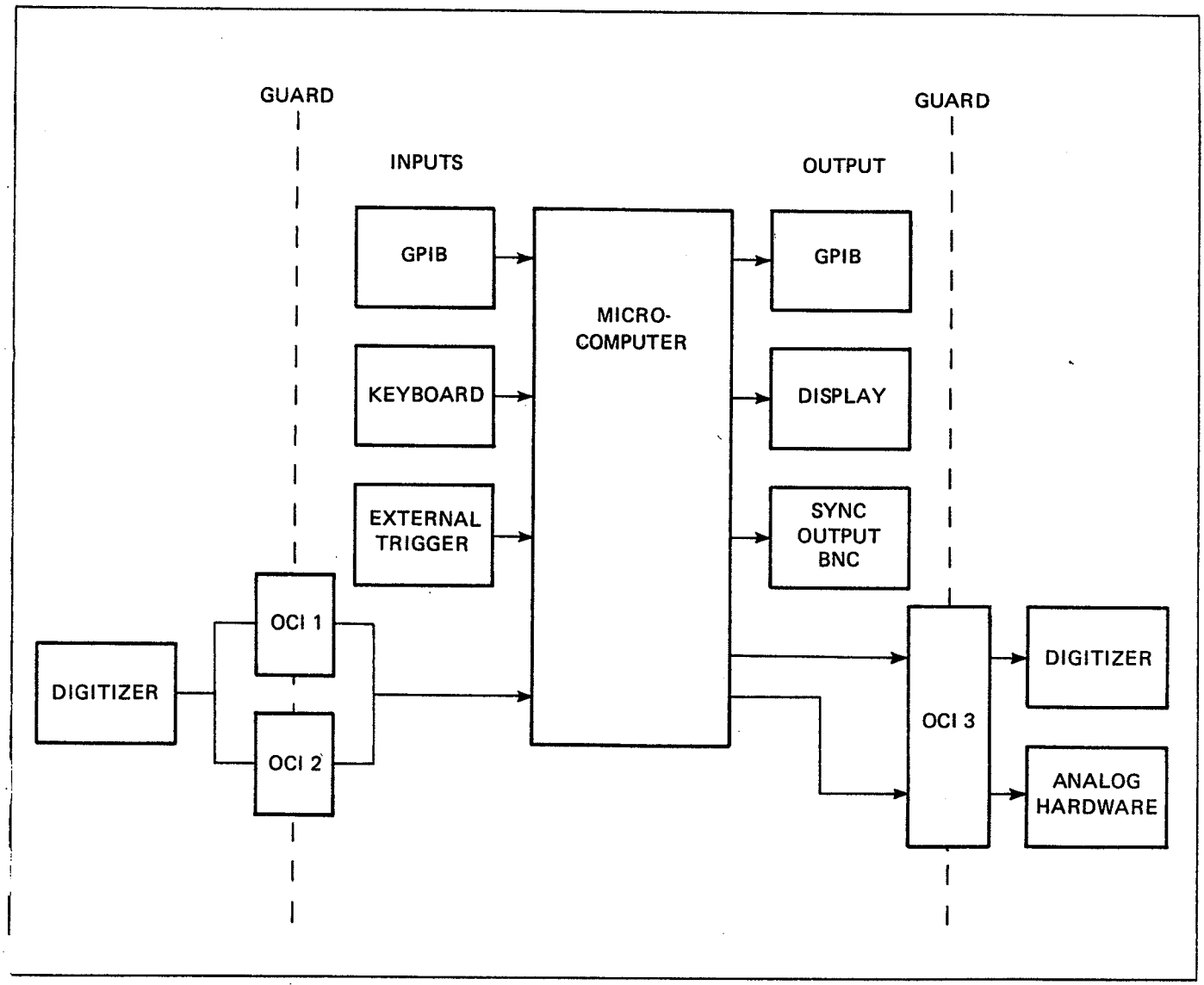


Figure 4.13 - Main Inputs To And Outputs From The Microcomputer

with the system clock E, therefore the outputs are practically a consistent pulse of 516 ns.

4.5.5 Non-Volatile Memory.

4.5.5.1 The DMM uses a non-volatile memory (NVM) to store calibration (CAL) constants for later recall. The constants are stored during laboratory calibration and are recalled from the NVM whenever the DMM Function or Range is modified. The NVM is comprised of U43, a CMOS RAM, and Nand gate U42 along with a three volt lithium battery BT1, zener diode VR12, a constant current regulator Q21 and steering diodes CR17 and CR21.

4.5.5.2 NVM POWER SUPPLY

4.5.5.2.1 During normal DMM power-on operation, the NVM circuit receives +9 volts unregulated from the digital power supply. The current from the unregulated supply is regulated by Q21, a FET connected as a constant current source. This constant current (normally 7-13 ma) flows to ground through VR12, creating a stable + 5.6 volts at the anode of CR17. This + 5.6 volts causes CR17 to forward bias, and supplies approximately + 5 volts to the anode of CR21, to the Vcc connection, and to IC's U42 and U43. The presence of + 5 volts on CR21's cathode causes it to turn off, thus preventing battery charging.

4.5.5.2.2 During the AC power-off periods, battery BT1 causes CR21 to forward bias so that approximately 2.5 volts is available to power U42 and RAM U43. This same voltage reverse-biases CR17 which prohibits battery flow into the power supply.

4.5.5.3 NVM WRITE-PROTECT

4.5.5.3.1 A hardware Write-Protect circuit prevents accidental modification of the contents of RAM U43 during normal power-up operation. This circuit is comprised of R/W control gate U42, a 10K pull-up resistor R79 and CAL-switch S1 which is located behind the front panel, refer to Figure 3.1-54 for illustration. When the switch is open, pin 14 on RAM U43 constantly remains HI, which prevents any RAM "write" operation so that its contents cannot be modified. When the CAL switch is depressed, the μP can drive the WRITE pin on the RAM LO, enabling the U43 memory modification.

4.5.5.4 NVM POWER-DOWN PROTECT

4.5.5.4.1 A power-down to deselect circuit prevents loss of RAM U43 CAL constants during power-up, power-down, and power brown-outs. The circuit is comprised of U53, a voltage level detector, along with the voltage-divider resistors R85 and R86.

4.5.5.4.2 U53 is configured to detect voltage variations in the + 5 VA power supply. During power turn-on, the + 5 VA supply passes up through the + 4 volt level, causing the voltage at U53 pin 3 to pass through approximately 1.2 volts. When this occurs, U53 pin 4 switches from the "off" state and becomes a low resistance path to ground, causing a logical low at U42 pins 3, 4 and 5. U42 pin 6 then goes high, allowing chip-select pulses from the μP to proceed thru to U43 pin 1. When power is cycled off or a brown-out occurs, the voltage at U53 pin 2 falls below 1.2 volts and a logical low appears at U42 pin 6, thereby blocking any further chip select signals

4.5.6 Interrupt Control Hardware.

4.5.6.1 The interrupt signals to the μP are processed by the interrupt control hardware consisting of dual Flip-Flop U2, two NAND gates in U6, and 1/6th of inverter U7.

4.5.6.2 The interrupts from the Digitizer and GPIA are NANDED by U6-4, 5, 6 and inverted by U7-3, 4, to appear on the interrupt request (IRQ) pin of the μP U35-4. This ANDing either from the Digitizer via the lower half of U2 or an interrupt from the GPIA via pin U6-5 will cause an interrupt to be gated to the μP.

4.5.6.3 External Triggers from the rear panel BNC connector J202, drive pin U6-2 LO then are inverted by U6 causing a positive edge at pin U2-3. This trigger clocks a LO at pin U2-5 which will cause a non-maskable interrupt (NMI) to occur at the μP pin U35-6. This NMI will cause the μP to cease its present software calculations and act upon the external trigger. The number of triggers arriving at the μP determine whether the μP will re-enable the external trigger or not. Enabling the external trigger occurs by the μP pulling pin U2-4 LO momentarily. If this is done, that portion of U2 will be set so that a second external trigger can be received by the hardware. If this is not done by the μP as would be the case when many external triggers are received rapidly, then pin U2-5 will remain in a LO state until the μP decides to pull pin U2-4 momentarily LO to set that half of U2.

4.5.6.4 The Analog Interrupts which originate from the analog side of the DMM are used to clock the lower half of U2. These evenly timed interrupts occur every 6 ms (every 7.2 ms in 50 Hz DMM) and clock the lower half of U2 at pin 11. This causes pin U2-9 to go LO, which causes the μP's IRQ input to go LO. When the μP responds to this interrupt, it reads the output of U20, a hex three-state buffer. Since pin U2-9 is connected to pin U20-10, the μP can determine if the IRQ originated from U2 by examining the D7 output (pin 9) from U20. If U2-9 is found to be low, the μP applies a negative pulse to pin U2-10, which removes the IRQ.

4.5.6.5 The interrupts which occur approximately every 6 ms as a result of the clock on pin U2-11 are used by the μP to sequence the scanning of the keyboard and to check whether certain front panel LED's need up-dating. If problems are observed in any of these areas, then a correct clock into pin U2-11 should be verified.

4.5.7 The Hardware Control Codes.

4.5.7.1 The hardware which brings information from the analog section of the DMM to the digital section is presented in schematic drawing on page 6-11.

4.5.7.2 The eight signals entering from the left edge of schematic on page 6-11 are brought in from the analog section of DMM through the opto-isolator couplers OCI-1 and OCI-2 to the digital three-state hex buffer U16. Four of these are multiplexed (MUX) BCD data lines A, B, C, D lines. Via these lines, 6 digit MUX BCD data is brought across guard through the opto-isolators. The other four lines are single lines designated as follows:

a) POLARITY: This line indicates the polarity of the most recently completed reading.

b) 1 KHz: This lines supplies a 1 KHz frequency (0.833 KHz in 50 Hz DMM). The high-low transitions of the 1 KHz waveform are monitored by the μP to determine when a new BCD digit is being MUX across guard on the A, B, C, D lines.

c) DIGIT STROBE SYNC D6: This line is used to generate real-time interrupts to the μP which was described previously and to help MUX the sign (polarity) bit into the μP.

d) EOC: (END OF CONVERSION) This line changes state when a new reading has been completed. After crossing guard the EOC line is buffered by TTL Schmitt inverter (sections of U7) and is used to clock the input of the dual F/F at pin U8-11. When the F/F is clocked, the output pin U8-9 goes HI. This high output is read by the μP and indicates to the μP that a new reading is ready. The buffered output of the opto-isolator also goes, via U7 and U6 TTL buffer, to the display board and is used to drive the "sample" LED. Refer to Figure 3.1-56 for the sample LED location.

4.5.7.3 When operating on 5 1/2 digit mode, the μP spends considerable time waiting for a new reading to become available for process and display. It determines when a new reading is available by reading pin U8-9 via U13, the keyboard three-state hex buffer. When the μP reads U13-3 HI, it then knows that a new reading is available and it begins to read the six digits which are constantly MUX across guard through opto coupler OCI-2. The μP reads the MUX BCD pulses and other control lines through U16 a three-state hex buffer.

4.5.7.4 A typical set of waveforms are presented in Figure 4.14 as they would appear to the μP while reading the MUX BCD data from the analog section, crossing guard, to the input of U16. The μP uses the positive edge of the 1 KHz signal to indicate when it should read the next nibble of BCD data from U16 inputs. The μP uses the DIGIT STROBE SYNC D6 signal to indicate when the most significant digit is MUX across guard.

4.5.7.5 The LO DIGIT STROBE SYNC D6 signal also causes the "sign" bit to be substituted in place of the D bit at U16's input. This switching of the sign bit in place of the D bit is done via the wired OR connection between the open collector outputs of OCI2 pin 10 and OCI1 pin 15.

4.5.8 Analog Control Registers.

4.5.8.1 The analog control hardware is housed in sections 4, 5, and 6 on the motherboard. The principal schematic on page 6-8 presents a relay operation chart and circuit details. Outguard portions of the circuit are shown on page 6-11.

4.5.8.2 The analog control system is comprised of a 4 bit latch U32, two shift registers U33 and U34, two relay drivers U18 and U19, relays K1 through K13, Schmitt trigger U25 and fet driver U36, as shown in Figure 4.15.

4.5.8.3 The μP program controls the digitizer, function, and range relays through 3 registers, 2 of which U34 and U33 are located on the analog side of guard, with the third U32, located on the digital side of guard.

4.5.8.4 U32 is a 4 bit latch which is loaded from the μP's data and address bus. The output from U32 is used to load registers U34 and U33 as well as trigger the digitizer shown on schematic on page 6-9.

4.5.8.5 U34/U33 REGISTER LOAD.

4.5.8.5.1 The DMM's function, range and/or integrate time can be modified as a result of keyboard inputs, GPIB commands, or autorange. When this occurs, a new relay drive bit pattern is determined by the μP. This pattern is then shifted across guard one bit at a time. The timing of the drive bit pattern is shown in Figure 4-16, the Register Load Timing diagram.

4.5.8.5.2 The first bit of this pattern, along with other control signals is latched into U32 from the μP's data bus and address bus. After propagating through the relatively slow opto coupler OCI-3, the data bit appears at the 'D' input of U34, along with a LO signal at U34's clock input. The microprocessor then stores the first bit to U32 along with other control signals that after progating through the opto-coupler, the first data bit remains at U34's 'D' input along with a "HI" signal at U34's clock input, which causes the first data bit to be shifted into U34. The above sequence is repeated until all 16 bits have been shifted into U34 and U33, which requires about 20 milliseconds.

4.5.8.5.3 After shifting all 16 bits into U34 and U33 the μP then strobes the shifted bits into the output registers of U34 and U33. To do this the μP stores a control bit pattern to U32 which propagates through OCI-3 and places a high level on U34-1 and U33-1. About 2 ms later, the μP removes this signal.

4.5.8.5.4 The output bits from U34 and U33 then energize relays via the open collector drivers U18 and U19, control Isolator gain via U36, or control the digitizer.

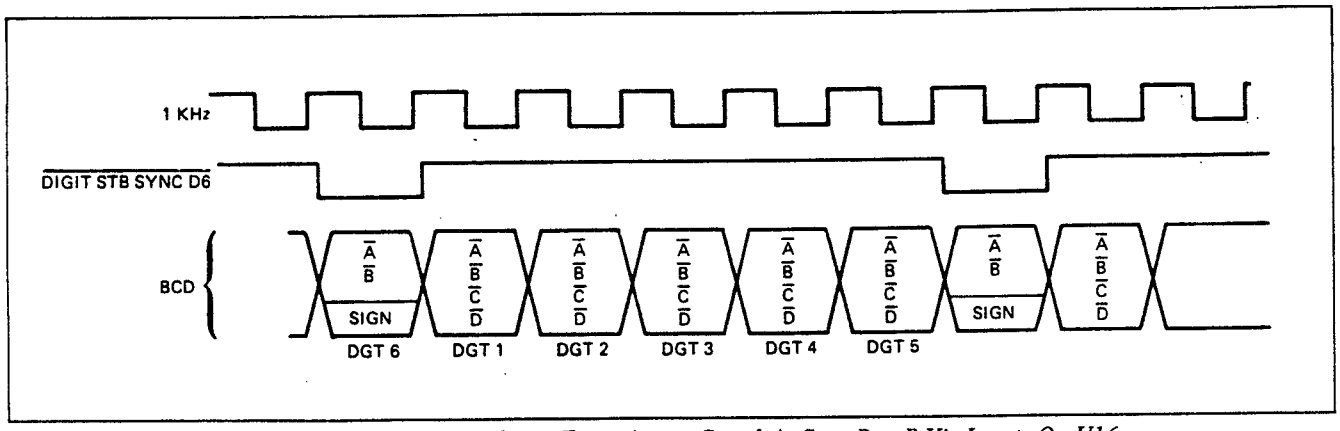


Figure 4.14 - Typical Waveforms From Across Guard As Seen By µP Via Inputs On U16

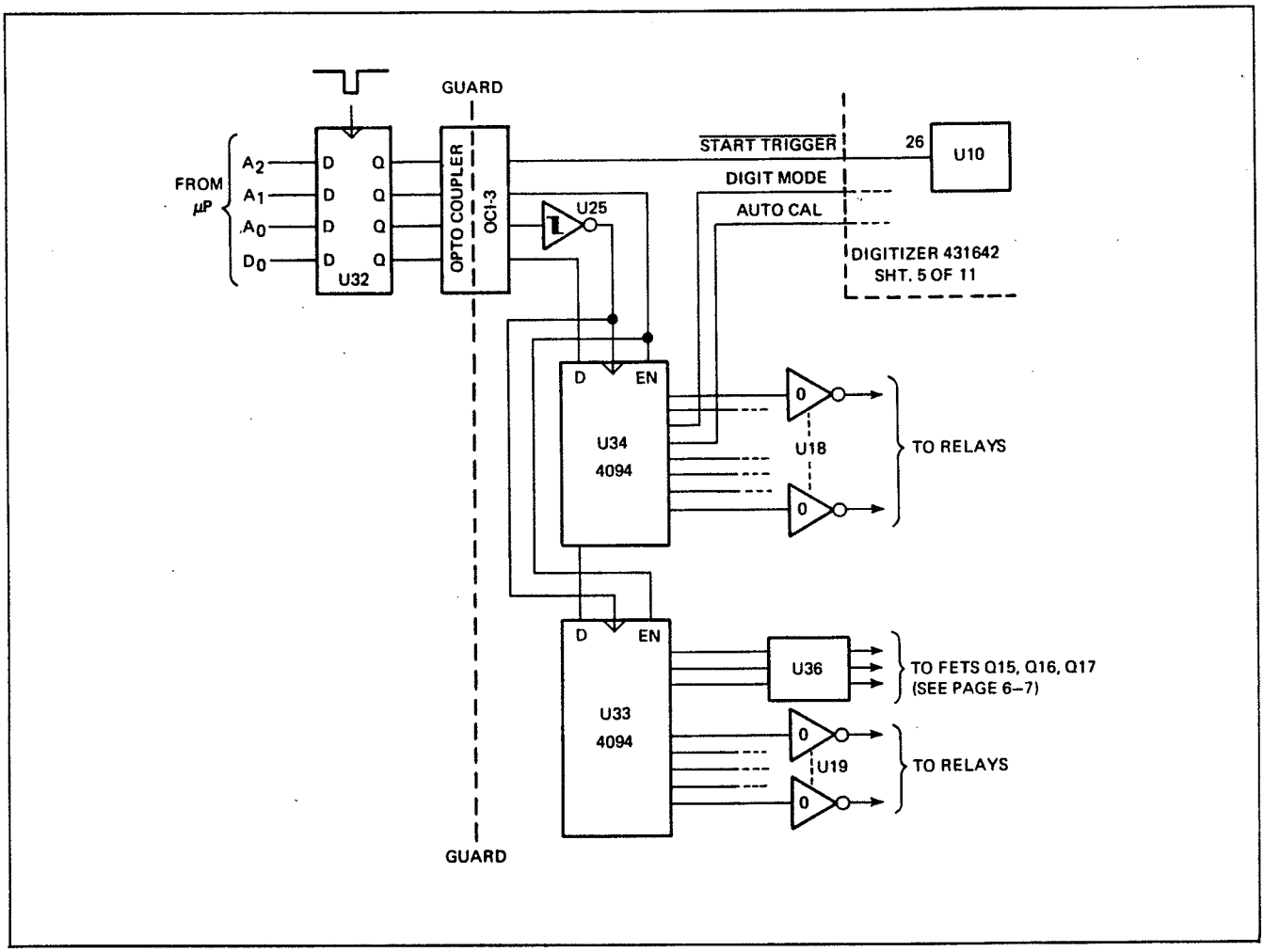


Figure 4.15 - Analog Control Registers

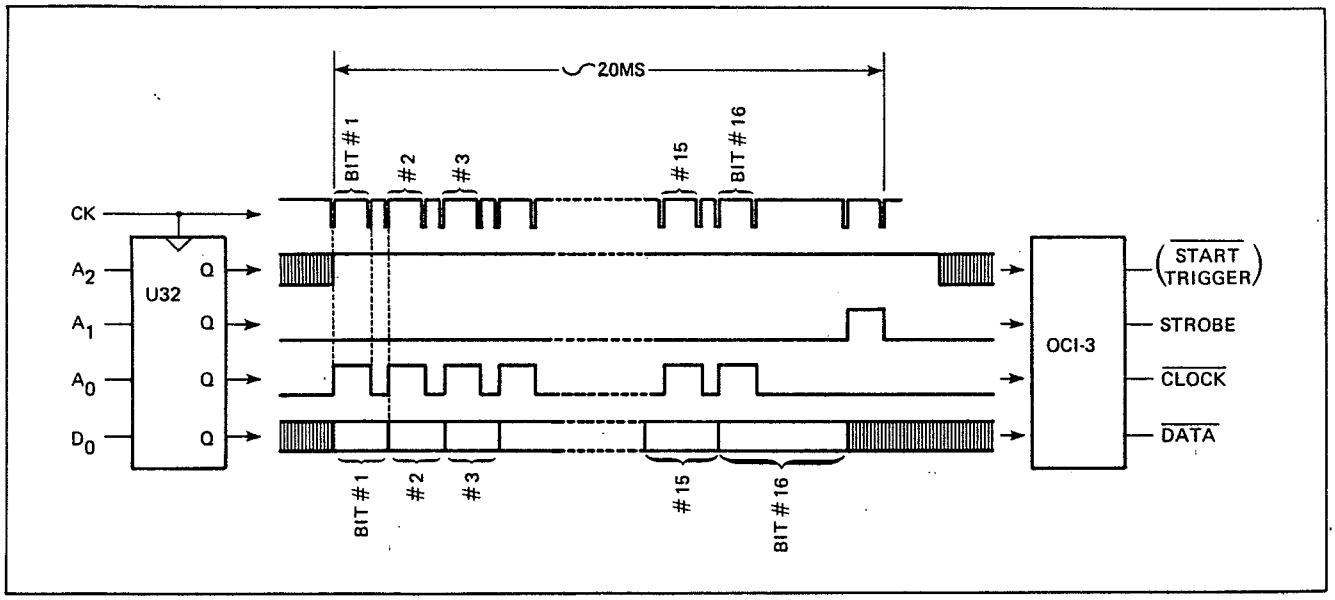


Figure 4.16 - Register Load Simplified Timing Diagram

4.5.8.6 DIGITIZER TRIGGERING.

4.5.8.6.1 When the μP requires a reading, it loads U32 with address line A2 LO. This then appears at U32's output, propagates across guard, and places a low level on pin 26 of U10 (digitizer drawing on page 6-9), to cause a read cycle.

4.5.8.6.2 When in the hold mode and at other times, the microprocessor waits for verification of a digitizer trigger by watching for a LO on pin 10 of U13, the keyboard buffer on page 6-14.

4.5.8.6.3 When operating in the "track" mode, (internal trigger) the μP leaves a LO on U10 pin 26 almost all the time in order to cause continuous triggers.

4.5.9 Keyboard Theory of Operation.

4.5.9.1 The DMM's keyboard is located on the display PCB whereas the associated ICs located on the motherboard; referred to as section 4 on the sectional chassis layout and detailed on schematic drawings on pages 6-14 and 6-17.

4.5.9.2 The keyboard circuitry consists of MB-U5, an open-collector inverter used to buffer the μP's address lines which drive the N, M, L, H, K, and J columns of the keyboard. The keyboard buffer U13 is a three-state buffer connected so that the μP can read the signal from the keyboard rows T, R, U, and S. The pull-up resistor network Z2 pins 3 through 6 ensures that the μP will read a HI from U13 if its inputs become open, a condition that exists when no key is pressed. The chip select for U13 is DSPE, which is the same chip select for U12. This chip select originates from the NAND gate output U6-8. See paragraph 4.6.3.1 for further explanation.

4.5.9.3 The OPERATION is described as follows. When the μP must determine if any key is pressed, it reads from U13 while address lines A0-A5 are high. The ones on A0-A5 lines propagate through U5 and appear as zeros on N, M, L, H, K and J columns of the keyboard as shown in Figure 4-14. When a key is pressed, the μP will read a zero on one of the row outputs through U13, the remaining rows will read ones. When a zero does appear, the μP then scans each keyboard column one-at-a-time by reading from U13 with only one of the lines A0-A5 high and others low, until the proper column has been driven low, and that a zero once again appears in the read from U13. Once this occurs, the μP suspends further keyboard scanning and processes the key in software.

4.6 DISPLAY BOARD.

4.6.1 Display Hardware.

4.6.1.1 The display hardware is configured on the motherboard (MB) as well as on the display board (Dspe). The LSI Display Controller and Driver MB-U12, 6-bit Range Latch MB-UI are located on the motherboard (MB). The display PCB contains the 7-segment LED read-outs DS1 through DS7. Function-Range-Status LEDs brightness-control current-limiting resistors and display drives V1, V2, and V3. This group occupies section 9 on the chassis.

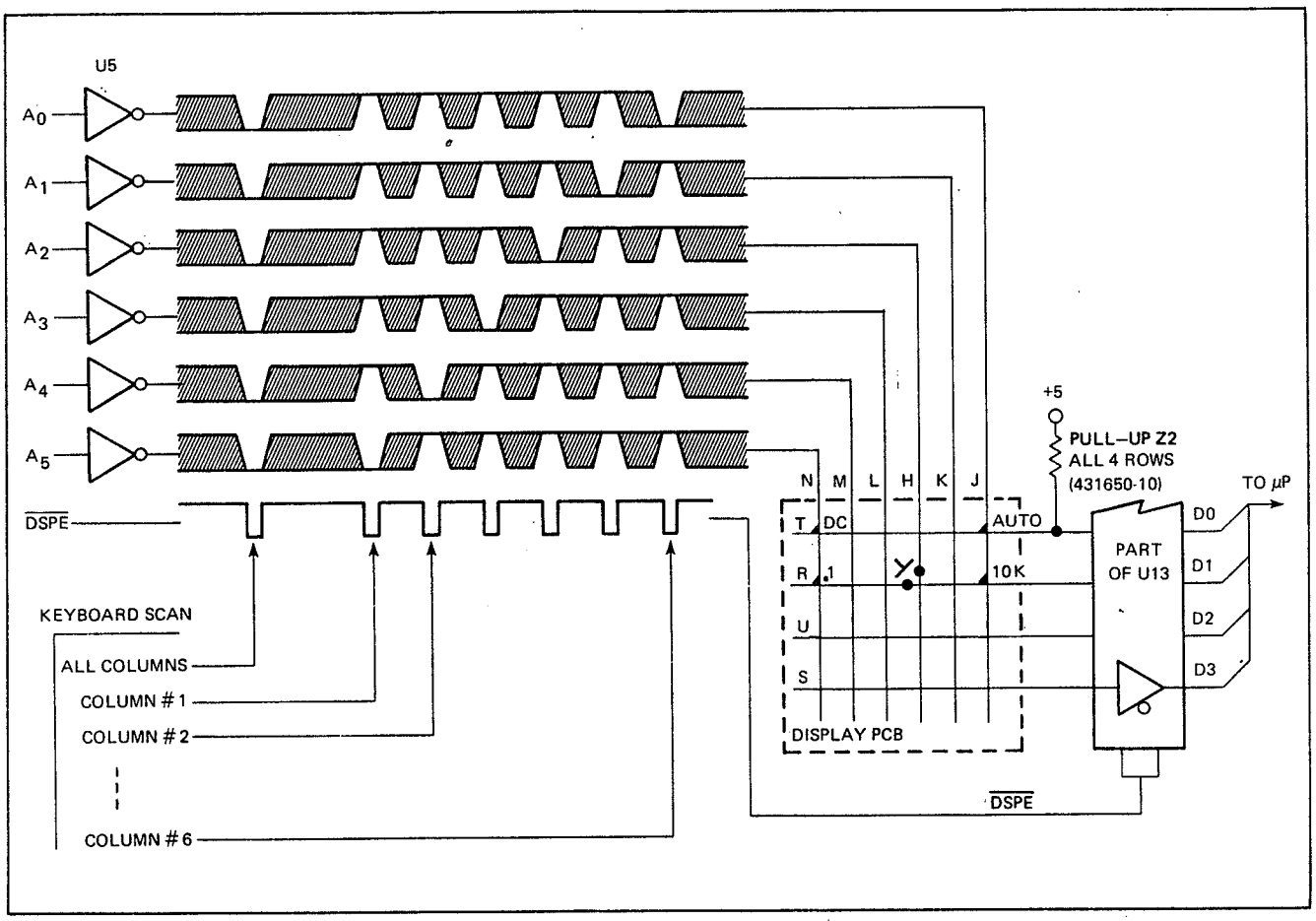


Figure 4.17 - Keyboard Block and Timing Diagram

4.6.2 Display Description.

4.6.2.1 The front panel LEDs are controlled by MB-U12 and MB-U1 through the μP. MB-U1 is a 6-bit latch which is loaded from the data bus by the μP. The outputs of MB-UI drive 5 range annunciator LED's and the "EXT REF" LED. The display configuration is presented in the block diagram Figure 4.18. This drawing merges the motherboard and display board components to give an overview of the display schematics on page 6-14 and the display control schematic on page 6-17.

4.6.2.2 The display device MB-U12 is an LS1 display controller with digit and segment drivers that execute the μP's LED bit pattern strobed through the multiplex scan circuitry. Dspe-U1 is a current sourcing driver which is used to buffer the display controllers column driver in the digit scan sequence. Dspe U2/U3 with associated resistors are current-sinking row drivers. The resistors R1 to R8 set the brightness level of the 7-segment and annunciator LEDs.

4.6.3 Operation.

4.6.3.1 The display controller shares a chip-select signal with the keyboard hardware. The AY2 output from the μP's address decoder U14 is effectively ORed with the μP's clock via pins U7-5/6 and pins U6-8/9/10, the resulting signal is called DSPE. This chip select is supplied as the negative read strobe to the keyboard and the negative write strobe to the display controller.

4.6.3.2 Whenever the μP wishes to update the LED pattern controlled by MB-U12, it latches a string of bytes into MB-U12 from the μP's address bus. The first of these is a byte which notifies the display controller that 8 data bytes will follow. The display controller differentiates between status bytes and data bytes by sampling the A8 address line during each write cycle (U12-9), which is high during status bytes and low during data byte writes. See Figure 4.19 for a simplified timing diagram.

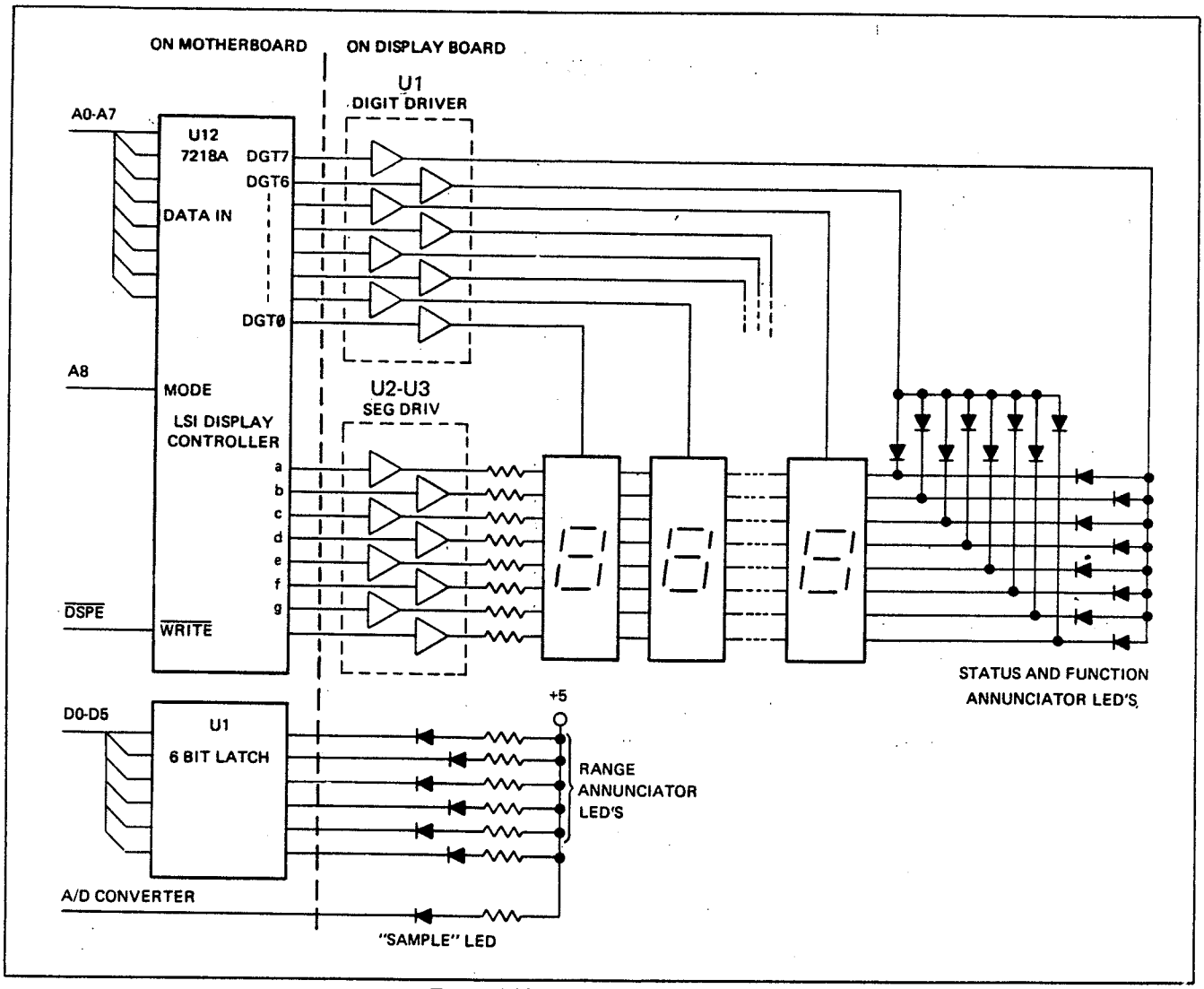


Figure 4.18 - LED Display Hardware

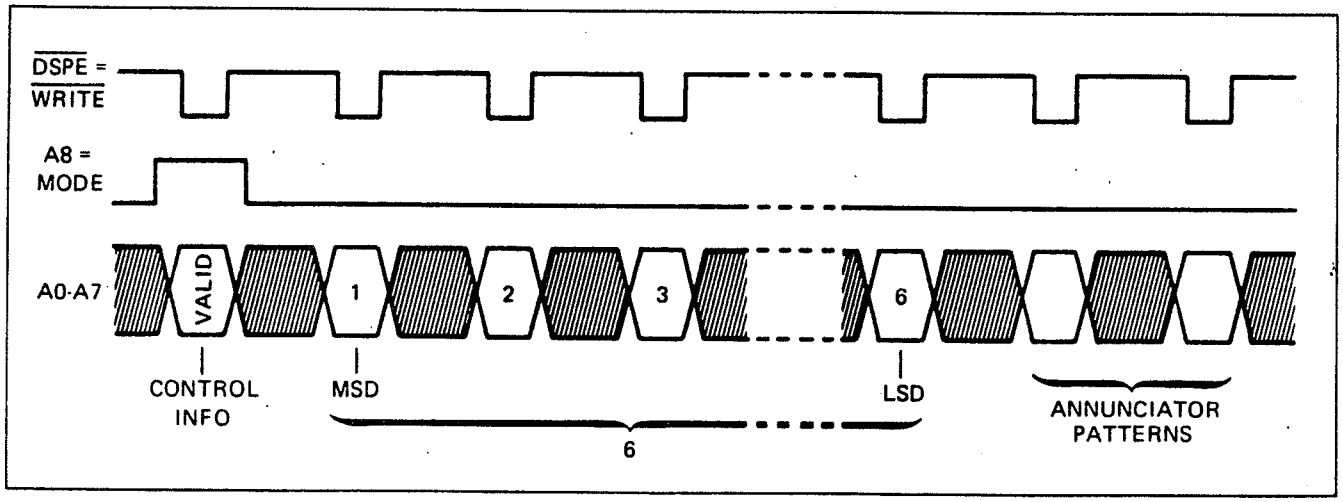


Figure 4.19 - µP Storage To LSI Display Controller Timing Signals

4.6.3.3 After all 8 data bytes have been latched into the display controller, it begins to refresh the 7-segment and annunciator LED's. To do this, the display controller first supplies an excitation MUX pattern to its row driver outputs a-g, which are buffered by DSPE U2/U3 and appear at the cathodes of all LED's. The display controller then turns on one column driver which, after being buffered by DSPE-U1, lights the appropriate LED's in that column. After a fraction of a millisecond, the controller turns off the column driver, changes the row excitation pattern, and turns on the next column driver, and so on. The LED refresh rate is fast enough that the human eye cannot detect the flicker.

4.6.3.4 The "Sample" LED located at the lower left corner of the decimal display is not controlled by U12 but instead, receives its control from the analog side of the instrument via U6-11 on page 6-11.

4.6.3.5 The brightness level for the Range LED's is set by the resistor network Z1 on the display PCB.

4.7 GPIB INTERFACE: THEORY OF OPERATION.

4.7.1 The DMM's IEEE-488 interface is centered around U44, the 68488 GPIA and positioned in section 8 on the motherboard. The other interface hardware in the GPIB Interface system include U46 and U47 bi-directional buffer/drivers; U37, U38 and U39 the Serial Poll Disable decoder; U45 the GPIA address switch buffer; and U40, U41 and U39 GPIA output holdoff circuit. These devices provide talker/listener capabilities, most interface commands and handle serial poll status bytes. The schematic for the GPIB hardware is listed on page 6-12.

4.7.2 The GPIA interfaces to the GPIB bus via U46 and U47 which are bidirectional octal GPIB transceivers. The U46/U47 data direction signal is controlled by the GPIA transmit/receive (T/R2) signal, from pin U44-27. The GPIA interfaces to the μP through 14 registers inside the GPIA which are accessed over the μP's data bus via GPIA pins U44-7 through U44-14.

4.7.3 The microprocessor's address and read/write lines are connected to the GPIA pins 37, 38, 39 and 5 to allow selection of the appropriate internal register by the μP. If the μP reads from the GPIA's register 4, the GPIA will not output data to the μP and will instead drive pin U44-4 low momentarily which will cause U45 to output the address switch setting to the microprocessor.

4.7.4 The GPIA handshakes most in-coming interface messages from the controller and acts upon them without disturbing the μP. If and when an incoming message or data byte requires a response from the μP, the GPIA drives its pin U44-40 low which sends an interrupt request IRQ to the μP via the interrupt control gate U6, which was previously discussed in paragraph 4.5.6. The μP then examines the GPIA's internal registers to release the IRQ and to determine the cause of the interrupt. The same interrupt sequence takes place if the GPIA is made a talker and has no byte to output.

4.7.5 The GPIB "Output Holdoff Circuit" was added between GPIA pin U44-18 and transceiver pin U47-7 to allow the μP more complete control to out-going bytes. This holdoff circuit has no effect except when the DMM is a talker, at which time it is used to pace the output of data and serial poll status bytes.

4.7.6 The GPIB Output Holdoff Circuit contains a 2-bit latch U40. The upper half of U40 is used to affect the output of all bytes while the lower half of U40 is dedicated to controlling the output of serial poll status bytes. U41 is a quad analog switch connected to U39 so that U40 is either enabling the passage of signals between pin U44-18 and pin U47-7 or U41 is forcing a zero on pinU44-18 to make the GPIA believe that no other 488-bus devices are ready for data.

4.7.7 The ICs U37, U38 and U39 pins 3 to 6 are used to decode the interface message "SPD" (Serial Poll Disable = hex 18) but since data on the bus is inverted, the logic must decode the complement of the SPD message. The output from this logic is OR'd with the single line GPIB message IFC (interface clear), inverted and supplied as the reset input to pin U40-13 so that pin U40-8 will be set back to its normal high state after a serial poll has been completed.

SECTION 5 MAINTENANCE

5.1 SCOPE.

5.1.1 The maintenance section includes specification checks, calibration procedures, and troubleshooting data required for routine service. Voltage measurements with waveforms tabulated under performance tests are supplied for troubleshooting guidance. A suggested equipment list is covered in Table 5.1. In addition, the program error message list is included with general troubleshooting information. The parts locator shown in Figure 5.4 is a reproduction of the PCB. All component references throughout the Maintenance Section are plainly noted on this drawing.

5.2 SPECIFICATION CHECK.

5.2.1 Scope.

5.2.1.1 This section contains procedures that compare the operation of the instrument against the published specifications presented at the front of this manual. It is intended to be used for incoming inspection and as a periodic check to determine if the calibration of the instrument meets published specifications. The procedures provide sufficient checks to verify proper operation and that the instrument is within the 6 month accuracy limits. The required ambient temperature of the environment is 23 ± 5 degrees centigrade.

5.2.2 Required Equipment.

5.2.2.1 A list of equipment is given in Table 5.1. The specific types of equipment suggested are listed under the Suggested Equipment heading. This list provides a guide for selecting suitable equipment having characteristics equal to or better than the items listed.

5.2.3 DC Voltage Sources.

5.2.3.1 To produce voltage levels of necessary accuracy, special techniques are required. Suitable methods of generating these voltages are shown in Figure 5.1. Tables 5.2 and 5.3. A precise and traceable source of 10 volts is required, not only for calibrating the 10 volt range, but

Table 5.1 - Required Equipment

Function	Qty	Item	Minimum Use Specifications	Suggested Equipment
DC	(1)	Saturated Standard Cell Bank (6 cells)	1 ppm, certified	EPPLEY 106
	(2)	DC Voltages Sources	0.1 ppm resolution	FLUKE 332B
	(2)	Voltage Dividers, Adjustable	< 1 ppm linearity	FLUKE 720A
	(1)	Decade Resistance Box		ESI DB62
	(2)	Null Detector/μ Voltmeters	1 μV sensitivity	FLUKE 845AR
AC	(1)	Thermal Transfer Standard	50 ppm	HOLT 6A, With corrections
	(1)	AC Voltage Source	1 ppm resolution	FLUKE 5200A/5215A
Ω	(8)	Resistance Standards	Known within:	
		100Ω	30 ppm	ESI SR1 with corrections
		1 KΩ	30 ppm	ESI SR1 with corrections
		10 KΩ	30 ppm	ESI SR1 with corrections
		100 KΩ	30 ppm	ESI SR1 with corrections
		1 MΩ	30 ppm	ESI SR1 with corrections
		10 MΩ	30 ppm	ESI SR1 with corrections
OTHER	(1)	Momentary Switch, SPST	–	–
	(2)	1.5 volt cells w/screwtype binding posts	–	–
	(1)	Insulated Adjustment tool	–	JFD5284
	(1)	100Ω, 10 Kilohm, 1 Megohm 1/4 Watt 5% Carbon Resistors	5%	–
	(1)	1 μFD non polar capacitor	–	–

Table 5.2 - DC Source and DMM Accuracies

Range	10 Volt Source	Voltage Divider	Total Accuracy	24 hr. DMM Full Scale Accuracy	Times Better
10	10 ppm	–	10 ppm	100 ppm	10
1	10 ppm	1 ppm	11 ppm	100 ppm	9
100mV	10 ppm	1 ppm	11 ppm	100 ppm	9
100	10 ppm	1 ppm	11 ppm	100 ppm	9
1000	10 ppm	1 ppm	11 ppm	100 ppm	9

also as a reference for generating highly accurate .1, 1, 100, and 1000 volt levels. The 10 volt source used must satisfy the following requirements.

a. It must be traceable to the National Bureau of Standards;

b. It must have a total accuracy of ±10 ppm;

c. It must have a low output impedance.

5.2.3.2 A source filling these requirements is shown in Figure 5.1. This circuit consists of a null detector, 7-decade voltage divider, a DC voltage supply, and a bank of saturated standard cells. Two advantages of this particular hookup are that; (a) there is minimal loading of the standard cells and (b) stability, not accuracy, is the primary requirement of the DC voltage supply. The output of this circuit is set to a precise 10 volts by setting the voltage divider to the value of the standard cells. The DC voltage source is then adjusted to produce a null on the null detector. The accuracy of the 10 volt source is within ±10 ppm. The remainder of the DC sources can be generated by the circuits shown in Table 5.4 and 5.5. Each of these hookups use a calibrated 10 volt source having the characteristics of the one previously described.

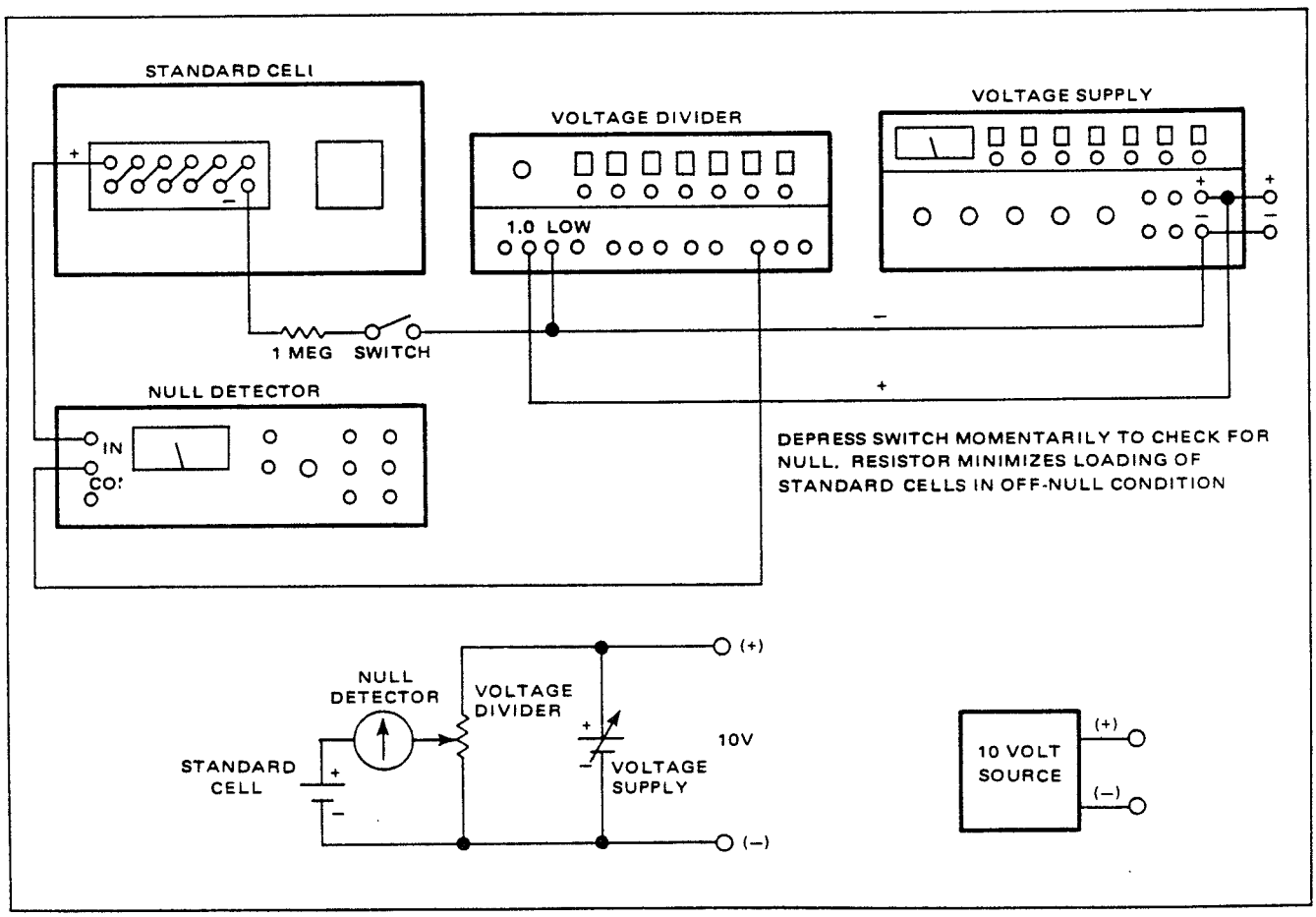


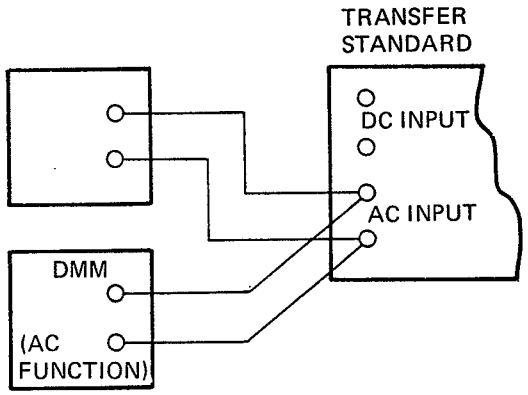
Figure 5.1 - 10 Volt Source

5.2.4 DC Accuracy.

5.2.4.1 The accuracy of the DC voltage sources is obtained by adding the various sources of error in each hookup; errors in this discussion are defined in parts per million (ppm). In Table 5.2 is shown the errors of each voltage source, the total accuracy of each hookup, the accuracy of the DMM, and the degree to which the sources exceed the required accuracy of the DMM (4 to 10 times better is the suggested accuracy ratio per MIL-M-38793).

5.2.5 AC Voltage Sources.

5.2.5.1 The generation of accurate AC signals for checking the AC converter ranges, requires the use of a thermal transfer standard and a precise DC standard as well as a stable AC source. Sufficient accuracy can be obtained by using a DC source and the DMM under test. The circuitry connections are shown in Figure 5.2. Information on the use of the transfer standard can be obtained from the operator's manual accompanying the standard. The DMM is used to set the DC source to the desired voltage and the thermal transfer is used to calibrate the output of the AC source. The calibrated AC source is used to check the DMM AC Converter. This procedure is repeated for each range.



The ac source is adjusted to produce a null on transfer standard. The ac source output is now calibrated and can be used as a precision source for the recalibration of the AC Converter.
NOTE: Because of the low input impedance of the transfer standard, the DMM input leads must be connected as close to the transfer standard input terminals as possible.

Figure 5.2 - AC Source

5.2.5.2 AC ACCURACY

5.2.5.2.1 The accuracy of the AC source is equal to the sum of the transfer-standard accuracy and the accuracy of DC source. The accuracy of the setup for each range and frequency used is provided in Table 5.3.

Table 5.3 - AC Source Accuracies

INPUT		ACCURACY		
AC Source		Thermal Transfer Standard	DC Source	Total AC Source
Volts	Freq			
1, 10, and 100 Volts	400 Hz	35 ppm	10 ppm	45 ppm
	50 kHz	50 ppm		60 ppm
500 Volts	40 kHz	50 ppm		60 ppm
1000 Volts	400 Hz	52 ppm		62 ppm

5.2.6 Test Procedures.

5.2.6.1 Allow two hours for warmup. Connect the instrument and the test equipment as shown in the figure supplied with each accuracy check. Select the controls and inputs as called out in the tables and monitor the instrument readout for the indicated values. Proceed with the tests described in Tables 5.4 through 5.9.

WARNING

The following procedures include the use of high voltage sources producing potentially lethal voltages. Avoid contact with high voltage terminals.

5.3 CALIBRATION.

5.3.1 This instrument was calibrated to published specications in Racal-Dana test Labs prior to shipment. The procedures in this section are designed to maintain calibration and keep the instrument operating within specifications.

5.3.2 Required Equipment.

5.3.2.1 A list of equipment required for calibration is given in Table 5.1. The specific equipment types are given only as a guide. If substitutions are made, the substituted equipment must meet or exceed the specifications of the equipment listed.

5.3.3 DC & AC Voltage Sources.

5.3.3.1 See Sections 5.2.3, 5.2.4, and 5.2.5.

5.3.4 Calibration Principles.

5.3.4.1 Calibration procedure for the DMM utilizes microprocessor controlled adjustments. The calibration adjustments executed through the keyboard input or GPIB commands are the software method of setting correction factors.

5.3.4.2 The Non-Volatile Constants memory of the DMM enables the microprocessor to perform software calibrations. Inputs are applied to the DMM from the calibration standard and the reading is incremented or decremented via keyboard control or GPIB commands until the reading equals the input standard. During this process, the numeric constants for analog offset voltages and scale factor corrections are loaded into the Non-Volatile memory by the microprocessor (μP). These constants are then used by the μP to correct each DMM reading before display or readout to the GPIB.

5.3.4.3 In order to enter correction constants into the Non-Volatile memory, three conditions are required:

a. The correct input standard for the function and range selected is applied to the DMM.

b. The calibration switch (Cal-Sw) must remain depressed during the adjustment process.

c. A keyboard input or GPIB command is required to increment or decrement the reading to equal the input standard.

IMPORTANT REMINDER

KEYBOARD OR GPIB CALIBRATION COMMANDS ARE "NOT" EFFECTIVE UNLESS THE CAL-SW IS HELD IN THE DEPRESSED POSITION. NUMBERS ARE ENTERED INTO THE NON-VOLATILE MEMORY ONLY WHEN THE CAL-SW IS IN THE "DEPRESSED POSITION".

5.3.4.4 The Cal-Sw is a momentary contact switch accessible through an opening on the front panel (see Figure 3.1 No. 8 for location). The switch can be depressed by inserting an appropriate size screwdriver or similar tool through the opening.

5.3.4.5 The DMM Function, Range and Input Standard for each entry into the Non-Volatile memory is listed in Table 5.10. One offset correction factor is entered for each Function and a scale factor is entered for each Range. In the DC Function, scale factors are entered for both positive and negative inputs, additionally a scale factor correction constant is entered for the 4 1/2 digit mode.

Table 5.4 - DC Function Check (Low Ranges)

DVM		INPUT SIGNAL		NOMINAL READING	TOLERANCE (6 MO. SPEC.) 5-1/2 DIGIT MODE	NOTE
FUNCTION	RANGE	DC VOLTAGE STANDARD	VOLTAGE DIVIDER SETTING			
DC	.1V	10.00000	.01000	.100000	.099974 – .100026	23°C ± 5°C (After DIGITAL ZERO Command)
		10.00000	.02000	.200000	.199954 – .200046	
	1V	10.00000	.10000	1.00000	.99984 – 1.00016	
		10.00000	.20000	2.00000	1.99974 – 2.00026	

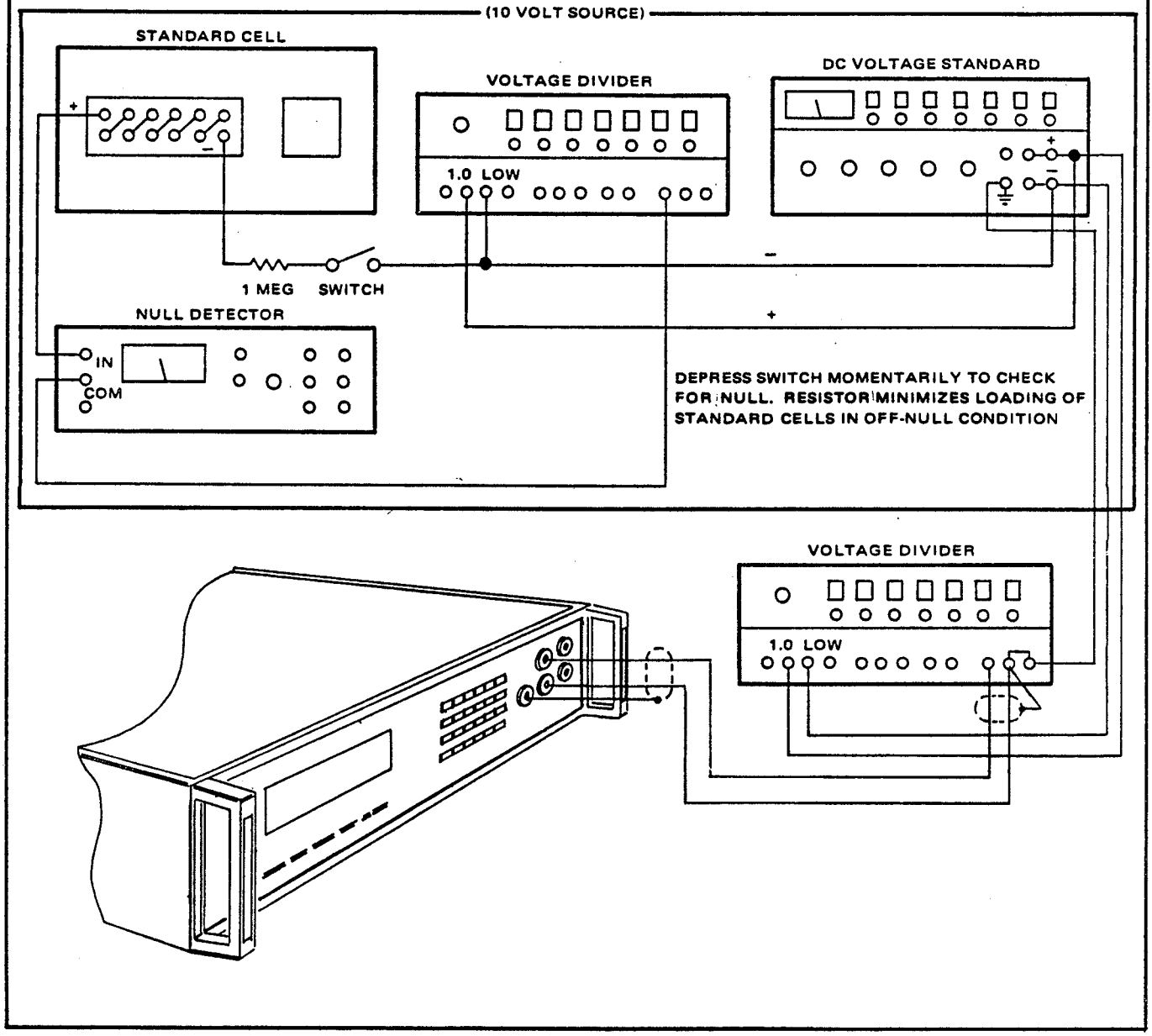


Table 5.5 - DC Function Check (High Ranges)

DVM		INPUT SIGNAL		NOMINAL READING	TOLERANCE (6 MO. SPEC.) 5-1/2 DIGIT MODE	NOTE
FUNCTION	RANGE	DC VOLTAGE STANDARD	VOLTAGE DIVIDER SETTING			
DC	10	10.0000V	1.0000	10.0000	9.9974 – 10.0026	23°C ± 5°C (After DIGITAL ZERO Command)
		20.0000V	.50000	20.0000	19.9954 – 20.0046	
	100	100.000V	.10000	100.000	99.974 – 100.026	
		200.000V	.05000	200.000	199.954 – 200.046	
	1000	1000.00V	.01000	1000.00	999.74 – 1000.26	

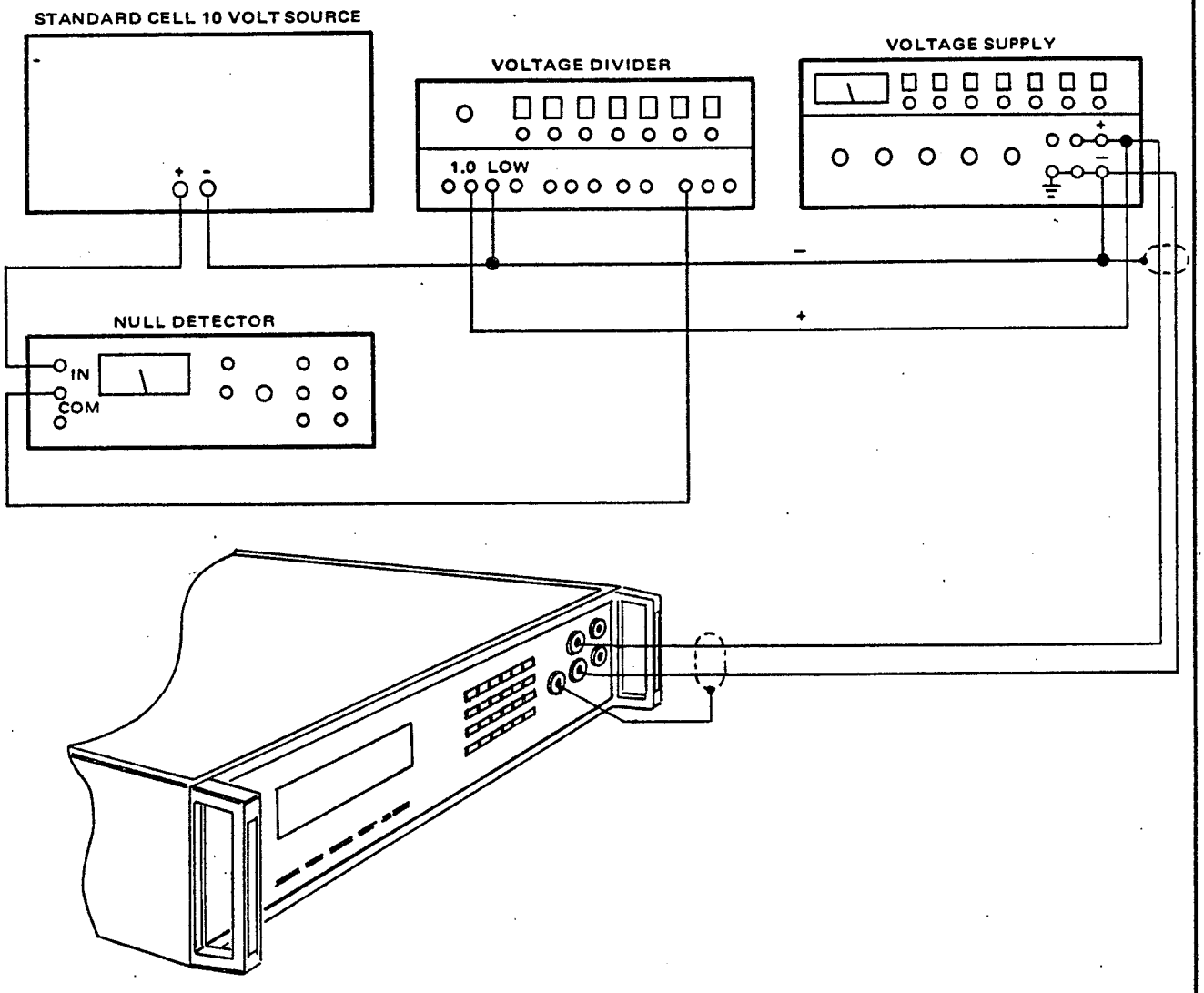


Table 5.6 - Averaging AC Converter Range Check Model 5005

DVM		INPUT SIGNAL		NOMINAL READING (5-1/2 Digit Mode)	TOLERANCE	NOTE (6 Month Spec)
FUNCTION	RANGE	DC VOLTAGE STANDARD	AC			
AC	1	1.000000	1V @ 400 Hz	1.00000	.99880 – 1.00120	23°C ± 5°C (After Auto Cal) *
		1.000000	1V @ 50 kHz	1.00000	.99830 – 1.00170	
	10	10.00000	10V @ 400 Hz	10.0000	9.9880 – 10.0120	
		10.00000	10V @ 50 kHz	10.0000	9.9830 – 10.0170	
	100	100.0000	100V @ 400 Hz	100.000	99.880 – 100.120	
		100.0000	100V @ 50 kHz	100.000	99.830 – 100.170	
	1000	1000.000	1000V @ 400 Hz	1000.00	997.80 – 1002.20	
		500.000	500V @ 40 kHz	500.00	498.55 – 501.45	

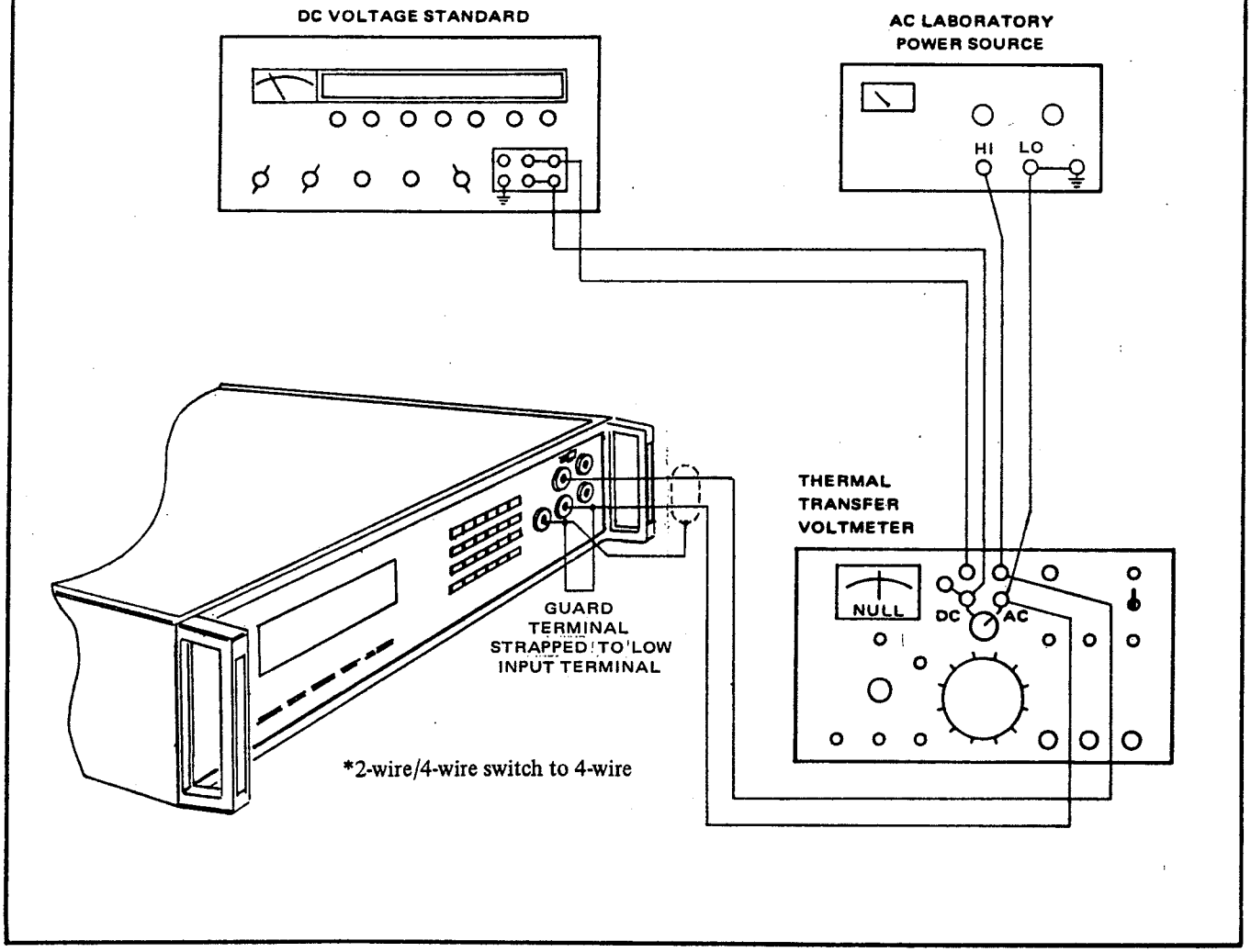


Table 5.7 - RMS AC Converter Range Check (Model 5006)

DVM		INPUT SIGNAL		NOMINAL READING (5-1/2 Digit Mode)	TOLERANCE	NOTE (90 Day Spec) (AC Coupled)
FUNCTION	RANGE	DC VOLTAGE STANDARD	AC			
AC	1	1.000000	1V @ 400 Hz	1.00000	.99840 – 1.00160	23°C ± 5°C (After Auto Cal) * Add ± 20 digits to spec if DC coupled mode is selected on AC Converter
		1.000000	1V @ 50 kHz	1.00000	.99800 – 1.00200	
	10	10.00000	10V @ 400 Hz	10.0000	9.9840 – 10.0160	
		10.00000	10V @ 50 kHz	10.0000	9.9800 – 10.0200	
	100	100.0000	100V @ 400 Hz	100.000	99.840 – 100.160	
		100.0000	100V @ 50 kHz	100.000	99.800 – 100.200	
	1000	1000.000	1000V @ 400 Hz	1000.00	997.40 – 1002.60	
		500.000	500V @ 40 kHz	500.00	498.00 – 502.00	

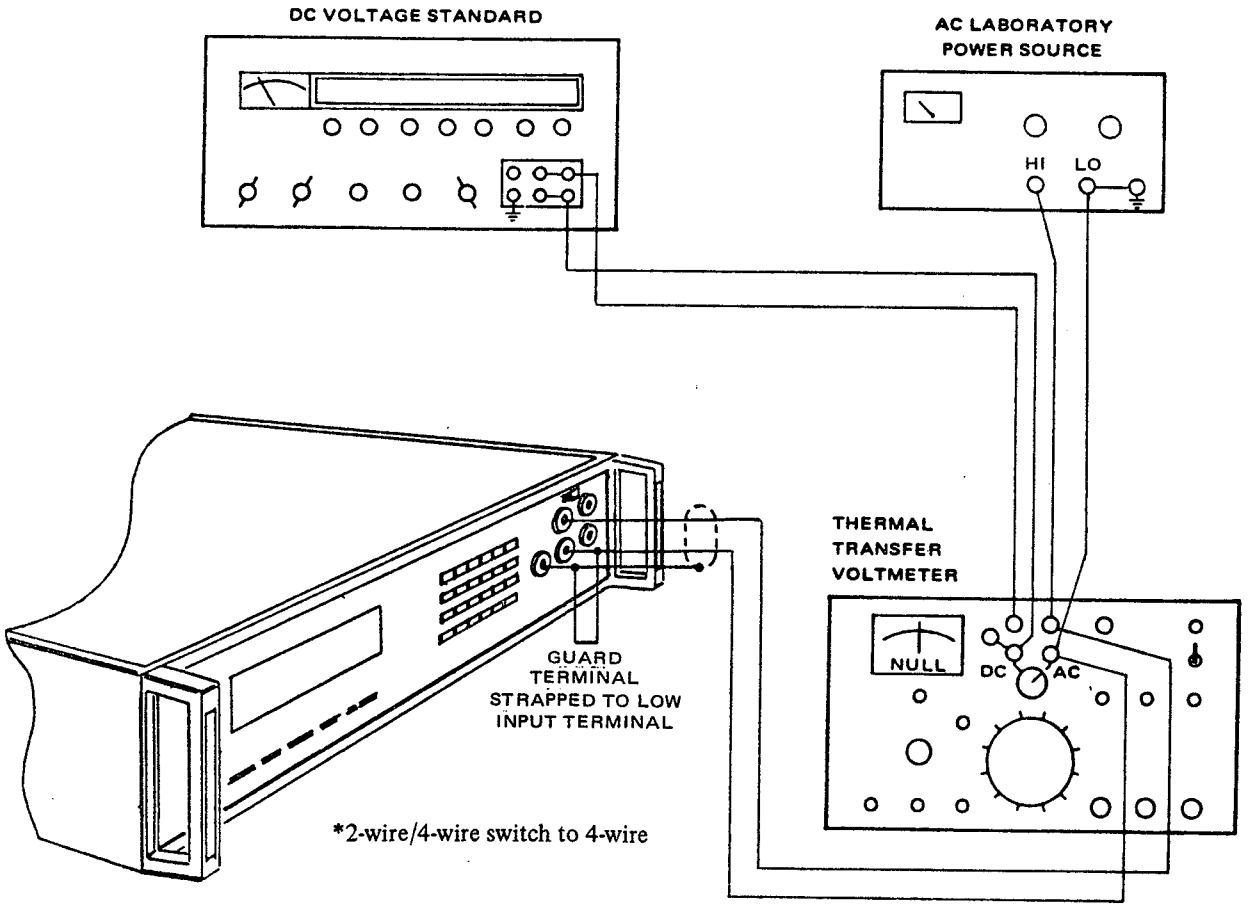


Table 5.8 - K Ohms Function

DVM		INPUT SIGNAL		TOLERANCE* (6 MO. SPEC.) 5-1/2 DIGIT MODE	NOTE
FUNCTION	RANGE	NOMINAL STANDARD VALUE			
KΩ	.1KΩ	100Ω		± 110 digits	23°C ± 5°C
	1 KΩ	1 KΩ		± 110 digits	
	10 KΩ	10 KΩ		± 110 digits	
	100 KΩ	100 KΩ		± 110 digits	
	1000 KΩ	1 MΩ		± 110 digits	
	10000 KΩ	10 MΩ		± 110 digits	

*After DIGITAL ZERO Command.

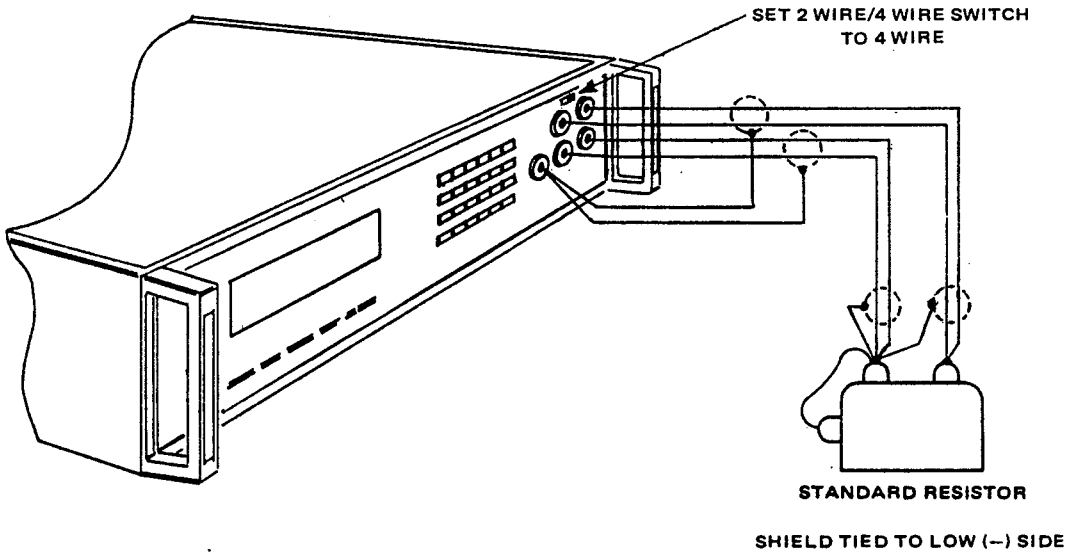


Table 5.9 - Normal Mode Noise Rejection (In DC Volts Function)

DVM		INPUT SIGNAL		NOMINAL READING	TOLERANCE	NOTE
FUNCTION	RANGE	DC	AC			
DC	10	0.5V	7.07V RMS 60 Hz*	00.5000	± 100 digits	

*50 Hz for 50 Hz Instruments.

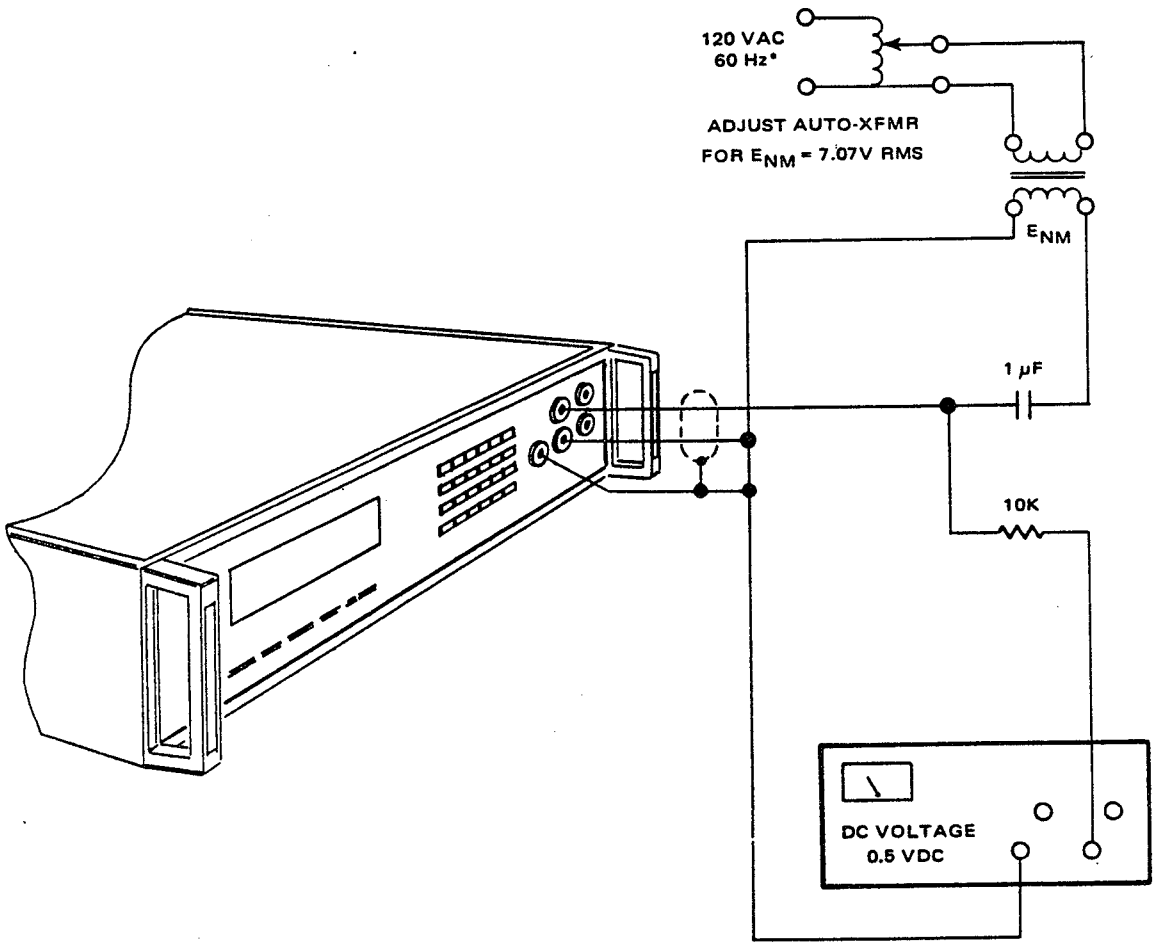
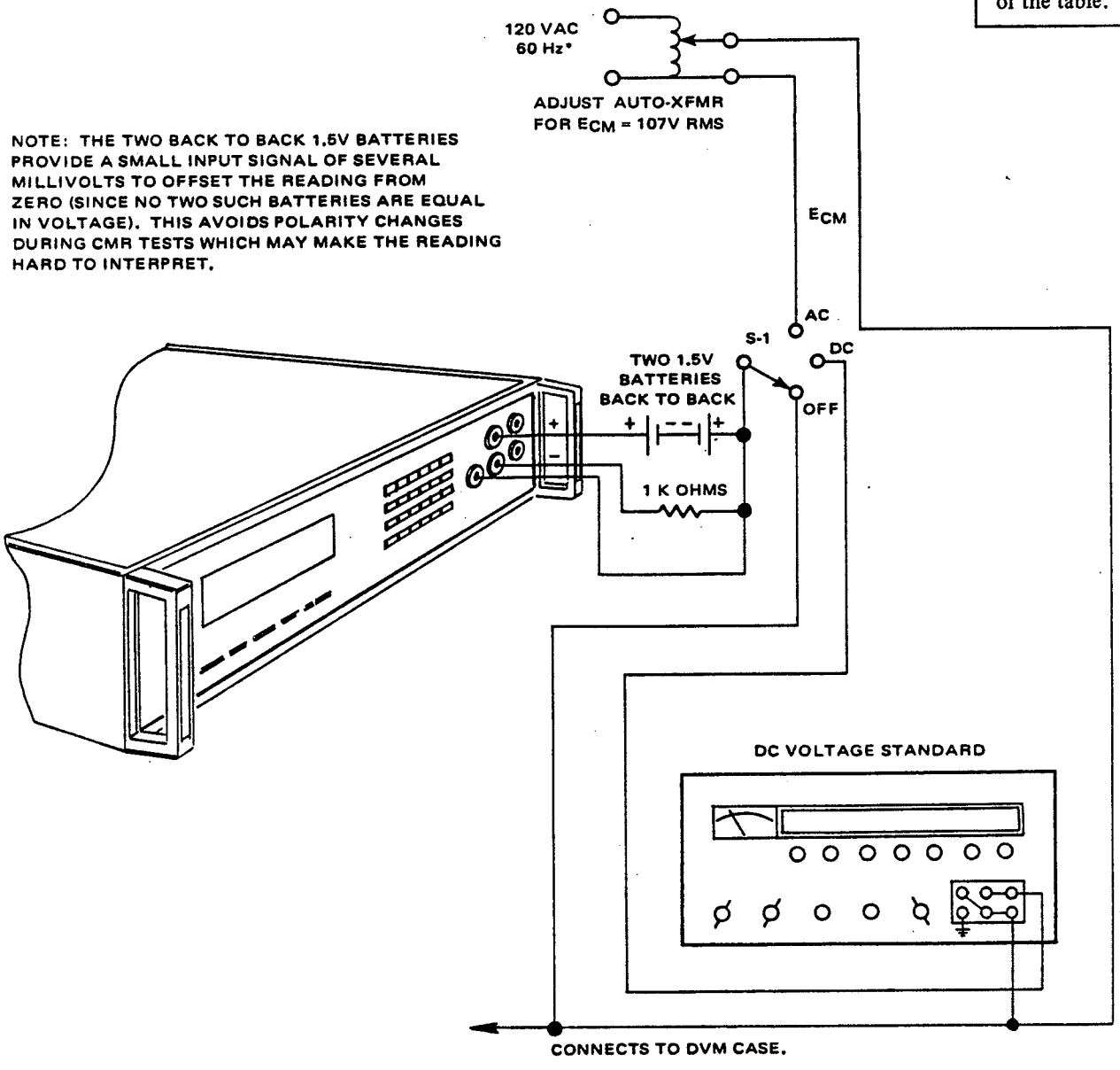


Table 5.10 - Common Mode Rejection (In DC Volts Function)

DVM		INPUT SIGNAL		NOMINAL READING See Note 1	TOLERANCE	NOTE
FUNCTION	RANGE	S1				
DCV	1V	Off				1) With switch S-1 in the off position, record the reading displayed on the DMM's readout in the "nominal reading" boxes of the table.
		DC	1000V		± 10 digits from nominal	
		AC	107V RMS 60 Hz*		30 digits peak-to-peak	

*50 Hz for 50 Hz Instruments.



5.3.4.6 MANUAL CALIBRATION

5.3.4.6.1 The DMM procedure to enter corrections using the keyboard command is as follows:

a. Offset Correction Factors: Zero volts or ohms are applied to the DMM.

b. Scale Factor Corrections: A full scale input is applied in each Function and Range.

c. Three input keys on the keyboard which perform the UP count, DOWN count, and NOMINAL functions are described below.

1. UP Key: Performed by depressing the RECALL key and referred to as RECALL/UP. This key increments the numbers in memory while the Cal-SW is held depressed.

2. DOWN Key: Performed by depressing the STORE key and referred to as STORE/DOWN. This key decrements the numbers in memory while the Cal-SW is held depressed.

3. NOMINAL Key: Performed by depressing the RESET key and referred to as RESET/NOMINAL. This key initializes the numbers in memory while the Cal-SW is held depressed, as explained in the next paragraph.

5.3.4.6.2 The RESET/NOMINAL key is used to initialize the numbers in Non-Volatile memory. When this key is depressed and released, either a ZERO is entered into the Non-Volatile memory as an offset correction factor, provided the DMM input is less than 40% of full scale, or a ONE is entered into the Non-Volatile memory as a scale factor, provided the DMM input is greater than 40% of full scale.

5.3.4.6.3 The STORE/DOWN key decrements the numbers in the Non-Volatile memory. This action is described as follows:

a. When entering an offset correction factor, this key changes the reading in a "Negative going" direction. For example, if the DMM reading is .00023 for zero input in the DC function, each time the STORE/DOWN key is depressed and released, the reading will decrease one digit. Upon reaching .00000, calibration of the DC offset correction factors is complete. Further depression of this key will cause the reading to increase with a negative polarity indication.

Table 5.11 - Non-Volatile Memory Constants

Memory Constant	Calibration Conditions		
	Function	Range	Input
DC Offset	DC	0.1 V	Zero
.1V Pos. Scale Factor	DC	0.1 V	+ 0.1 V DC
.1V Neg. Scale Factor	DC	0.1 V	−0.1 V DC
1V Pos. Scale Factor	DC	1V	+1VDC
1V Neg. Scale Factor	DC	1V	−1VDC
10V Pos. Scale Factor	DC	10V	+10VDC
10V Neg. Scale Factor	DC	10V	−10VDC
100V Pos. Scale Factor	DC	100V	+100VDC
100V Neg. Scale Factor	DC	100V	−100VDC
1KV Pos. Scale Factor	DC	1KV	+1KVDC
1KV Neg. Scale Factor	DC	1KV	−1KVDC
4 1/2 Digit Scale Factor	DC	1V	±2VDC
AC Offset	AC	1KV	Zero
1V Scale Factor	AC	1V	1V RMS, 400 Hz
10V Scale Factor	AC	10V	10V RMS, 400 Hz
100V Scale Factor	AC	100V	100V RMS, 400 Hz
1KV Scale Factor	AC	1KV	1 KV, 400 Hz
Ohms Offset	KΩ	100K	Zero
.1KΩ Scale Factor	KΩ	0.1 K	100Ω
1KΩ Scale Factor	KΩ	1K	1KΩ
10KΩ Scale Factor	KΩ	10K	10KΩ
100KΩ Scale Factor	KΩ	100K	100KΩ
1000KΩ Scale Factor	KΩ	1000K	1MΩ
10,000KΩ Scale Factor	KΩ	10,000K	10MΩ

b. When entering scale factors, each depression of the STORE/DOWN key will decrease the displayed reading one digit when a Full Scale Input is applied.

c. When the decrements required for corrections are numerous, holding the STORE/DOWN key depressed longer than two seconds approximately, will decrement the readings as a faster rate as long as the key remains depressed.

5.3.4.6.4 The RECALL/UP key increments the numbers in the Non-Volatile memory. This action is described as follows:

a. When entering an offset correction factor, this key changes the reading in a "Positive going" direction. For example, if the DMM reading is −.00023 for zero input in the DC Function, each time the RECALL/UP key is depressed and released, the reading will decrease one digit. Upon reaching .00000, calibration of the DC offset correction factor is complete. Further depression of this key will cause the reading to increase with a positive polarity indication.

b. When entering scale factors, each depression of the RECALL/UP key will increase the display reading one digit as a Full Scale input is applied.

c. When the increments required for corrections are numerous, holding the RECALL/UP key depressed longer than two seconds approximately, will increment the readings at a faster rate as long as the key remains depressed.

5.3.4.6.5 In situations where the input standard and the initial reading differ by several hundred digits, the difference can be reduced at the fastest rate by switching to the 4 1/2 digit mode (depress and release RESOL key). In the 4 1/2 digit mode, each depression of the RECALL/UP or STORE/DOWN key changes the reading one digit, which is 10 digits on the 5 1/2 digit mode. Holding either key depressed for fast increment or decrement operation also changes the reading in 10 digit increments. Once the reading has been reduced to within a few digits of the input standard in the 4 1/2 digit mode, switch back into the 5 1/2 digit operation to complete the calibration.

5.3.4.6.6 When using the 4 1/2 digit mode to change the reading rapidly, the DMM "must be in a fixed range" (AUTO ranging disabled and AUTO annunciator OFF). When this precaution is not taken, the 4 1/2 digit Scale Factor will be modified instead of the desired Non-Volatile memory constant.

5.3.4.6.7 If the 4 1/2 digit Scale Factor is inadvertently modified, the 4 1/2 and 5 1/2 digit readings will differ. To re-initialize the 4 1/2 digit Scale Factor, the following procedure is presented.

a. Select the DC Function any Range, 4 1/2 digit mode, Auto-ranging (Auto-annunciator ON).

b. Apply a full scale input to the DMM for the Range selected in (a.).

c. Depress and hold the calibration switch.

d. Depress and release the RESET/NOMINAL key.

e. Release the calibration switch.

WARNING

These instructions are for use by qualified personnel only. To avoid electric shock, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so.

5.3.4.7 GPIB CALIBRATION

5.3.4.7.1 When calibration is performed via the GPIB, it is convenient to short the Cal-Sw terminals with a temporary jumper. The Cal-Sw drawing shown in Figure 5.3 indicates the location of the jumper.

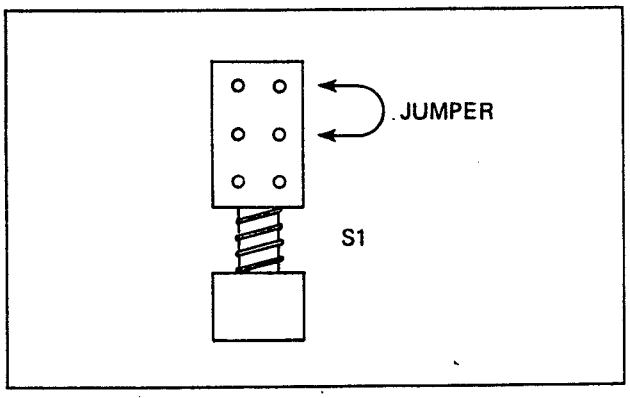


Figure 5.3 - Cal-Switch, Top View

IMPORTANT

Connect the jumper after power is applied to the DMM and disconnect the jumper before power is removed. If this instruction is not followed, the contents of the Non-Volatile memory will be destroyed and "Error 4" will be displayed the next time power is applied to the DMM.

5.3.4.7.2. GPIB commands K3 through K5 affect the Offset constant for the Function which is presently programmed. Each transmission of the K3 or K5 command to the DMM is equivalent to applying a low-level input (Low level is less than 40% and high-level is greater than 40% of Full Scale.), and momentarily pressing the STORE/DOWN or RECALL/UP keys on the DMM front panel. Transmitting the K4 command is equivalent to the keyboard procedure for initializing offset constants, with the exception that the input signal need not be less than 40% of full scale when initializing offset constants over the bus.

5.3.4.7.3 GPIB commands K6 through K8 affect the Scale constants for the range which is presently programmed. Each transmission of the K6 or K8 command to the DMM is equivalent to applying a high level input and momentarily pressing the STORE/DOWN or RECALL/UP keys on the DMM front panel.

5.3.4.7.4 Transmitting the K7 command has the same effect as initializing scale constants from the keyboard. To initialize a scale factor over the GPIB, the following procedure is provided:

a. Apply a high-level input signal.

b. Complete at least one reading on the presently programmed function/range.

c. Transmit the K7 command to the DMM.

> **NOTE**
>
> The K4 and K7 commands should not be required unless the contents of the non-volatile are destroyed.

5.3.5 Calibration Procedure.

> NOTE
>
> Initialize the non-volatile memory, as described in section 5.3.6, with "reasonable" Cal factors to prevent improper function of the Cal memory.
>
> If repairs were completed recently, refer to section 5.3.6 for instructions.

5.3.5.1 INPUT BIAS CURRENT NULL (R53).

a. Connect the Decade Resistance Box across the INPUT terminals. Select DC Function, .1V Range and FILTER.

b. Allow instrument at least one hour warmup with covers in place.

c. Switch Decade Resistance Box between 0 and 1 Megohm. If display changes more than ± 50 digits as Decade box is switched, proceed to steps (d.) and (e.).

> **WARNING**
>
> Removal of covers exposes potentially lethal voltages. Avoid contact with internal electrical connections while unit is connected to AC Power source.

d. Remove top cover for access to R53, but keep cover in place when not adjusting R53.

e. Adjust R53 until display changes less than ± 50 digits as Decade box is switched between 0 and 1 megohm. See Figure 5.8 for R53 location.

5.3.5.2 MODEL 5005 (AVERAGING AC PRE-CALIBRATION PROCEDURE

5.3.5.2.1 Model 5005 pre-calibration procedure reference drawings are shown in Figures 5.4 and 5.5. The procedures are described in the following paragraphs:

a) Set the DMM to AC and the 1V range.

b) Apply 100 mV at 400 Hz from the AC calibrator to the HI-LO Input terminals.

c) Adjust R19 on the AC-PCB (section 2-a) for minimum (most negative readout).

d) Refer to Figure 5.4 - a functional diagram, and Figure 5.5 - the component location of the AC converter.

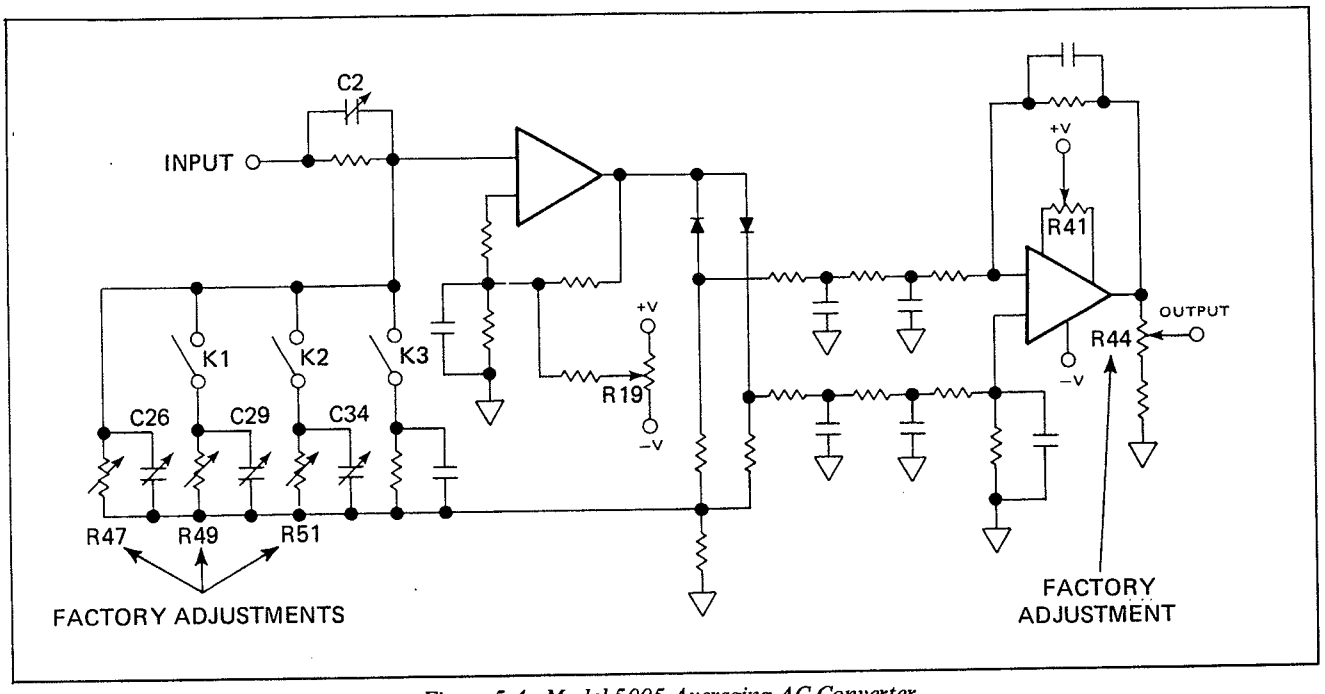


Figure 5.4 - Model 5005 Averaging AC Converter

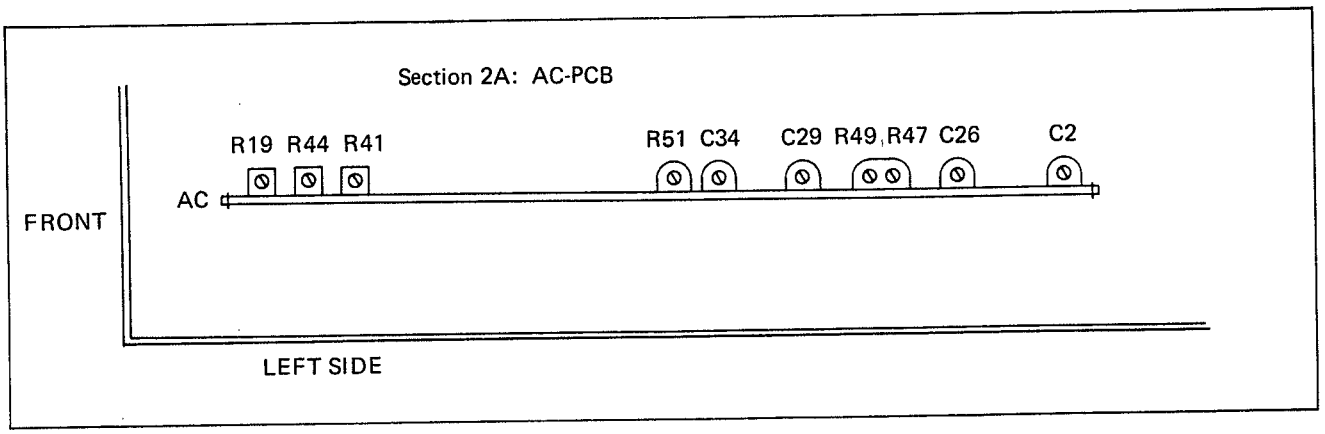


Figure 5.5 - Model 5005 Calibration Points

5.3.5.3 MODEL 5006 (RMS) AC PRE-CAL PROCEDURE

5.3.5.3.1 Model 5006 AC Pre-Cal procedure reference drawings are shown in Figures 5.6 and 5.7. The calibration procedures are described in the following instructions.

5.3.5.3.2 Select AC 1V range and short the DMM's input terminals together. Connect a micro voltmeter between TP6 (+) and TP1 (–) on the motherboard. If the microvoltmeter reading is greater than 0 ± 300 microvolts, perform the steps of the pre-cal adjustment procedure listed below.

a) Set DVM power switch to off. Extract converter and remote environmental shield. Set S1 and S2 to DC (toward center of board), replace converter and set power switch to on. Select AC and 1 volt range on DVM front panel. Allow 10 minutes for temperature to stabilize.

b) Connect jumper across DVM input terminals. Connect the microvoltmeter to TP2 (+) and TP5 (–). Adjust R17 for a microvoltmeter reading of 0 ± 30 μV. Remove + microvoltmeter lead from TP2. Turn R38 fully clockwise.

c) Connect microvoltmeter + lead to TP4.. Adjust R41 for a microvoltmeter reading of +20 ± 10 μV.

d) Connect + microvoltmeter lead to TP1. Adjust R28 for a microvoltmeter reading of 0 ± 30 μV. Remove microvoltmeter + lead from TP1.

e) Connect + microvoltmeter lead to TP3. Adjust R25 for 0 ± 30 mV. Remove + microvoltmeter lead from TP3.

f) Connect + microvoltmeter lead to TP4. Adjust R38 counterclockwise until the voltage at TP4 reads 0 + 5 μV. Remove microvoltmeter leads and remove jumper across DVM input.

g) Apply –1.00000V DC and note DVM display.

h) Reverse polarity of input to + 1.00000V DC and adjust R33 to obtain approximately the same DVM display as obtained in step g. Repeat steps g and h until the two readings are within .01% of each other. Remove DC supply from DVM input.

j) Reverse polarity of input to –0.100000 and verify DVM display is within + 5 digits of the reading obtained in step i. If not, use R25 to balance the readings. Select FILTER.

k) Set power switch on DVM to off, extract converter, set S1 and S2 to AC to their original position. Replace environmental shield on converter and replace converter in DVM. Reapply power and allow 10 minutes for temperature to stabilize.

5.3.5.4 "DIGITAL" CALIBRATION.

a. Verify that all shields and covers are installed.

b. Short the INPUT terminals and GUARD terminal together.

c. Allow at least 2 hours warmup with covers installed before proceeding.

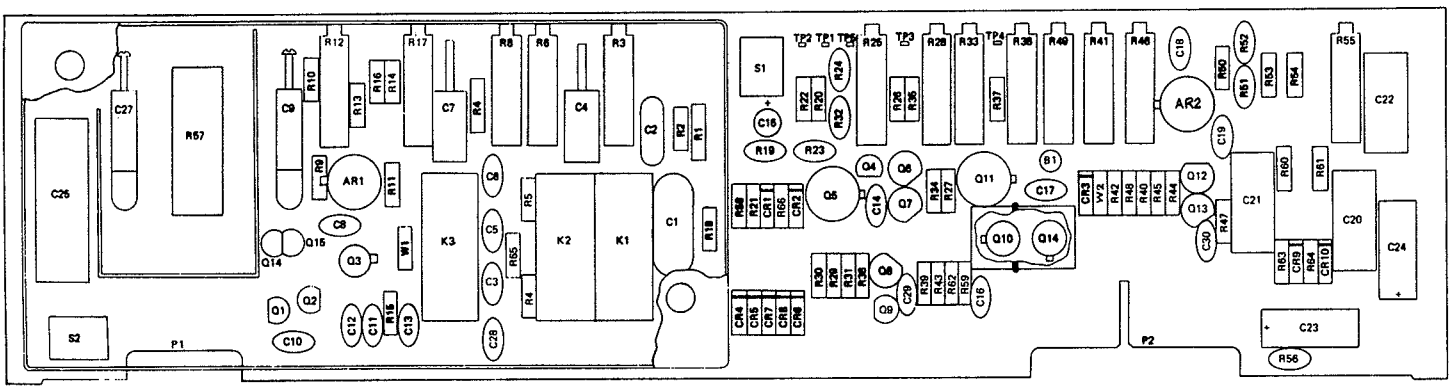


Figure 5.6 - RMS - PCB Assembly

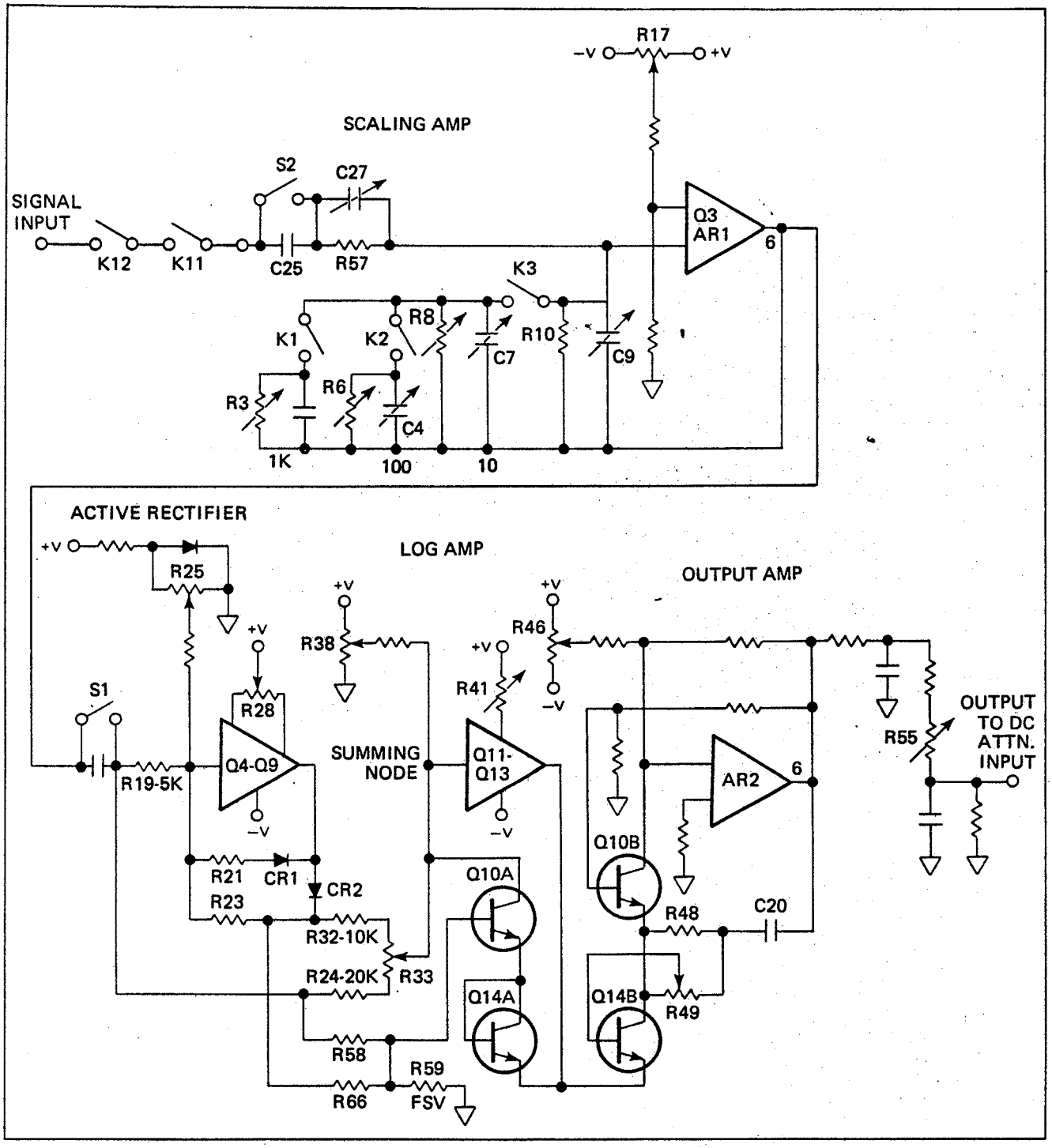


Figure 5.7 - Calibration Points

Table 5.12 - Calibration Points for Entry of Final Values Into Non-Volatile Memory

Function	Range	Input Standard	Input Connections	Notes
DC	.1V .1V .1V 1V 1V 1V	0.00000 VDC +0.1 VDC −0.1 VDC +1.0 VDC −1.0 VDC (Note 1)	Table 5.4	Note 1 - See paragraph 5.3.5.5 to calibrate 4 1/2 Digit mode.
	10V 10V 100V 100V 1KV 1KV	+10.0 VDC −10.0 VDC +100.0 VDC −100.0 VDC +1000.0 VDC −1000.0 VDC	Table 5.5	Note 2 - The value of the Resistance Standard must be known to within the tolerance indicated in Table 5.1.
AC	See Note 3 1V 10V 100V 1KV	See Note 3 1.0V RMS, 400Hz 10.0V RMS, 400Hz 100.0V RMS, 400Hz 1000.0V RMS, 400Hz	Table 5.6	Note 3 - Range, Input Standard and procedure varies: 5005: Range: 1KV Input Standard: 0.0 VRMS 5006: Apply 0.100VAC at 400Hz and calibrate using procedure in sections 5.3.5.6f thru 5.3.5.6j. Perform next calibration point (1.0VRMS) using same procedure. Repeat 0.1 VRMS and 1.0VRMS calibrations until both are within specifications.
KΩ	100KΩ .1KΩ 1KΩ 10KΩ 100KΩ 1000KΩ 10,000KΩ	0.0Ω 100.0Ω 1.0KΩ 10.0KΩ 100.0KΩ 1.0MΩ 10.0MΩ } Note 2	Table 5.7	

d. Select DC Function. Hold the .1V Range key depressed until "CAL 0" appears on the display, then release the Key.

e. Depress and hold the Calibration Switch.

f. Depress and release the RESET/NOMINAL Key.

g. Disable the Auto-range function by depressing the .1V Range Key. The AUTO annunciator will be OFF when disabled.

h. Refer to Table 5.12 for the Function, Range and Input for each calibration point. Verify that the AUTO annunciator remains OFF at each calibration point unless otherwise instructed.

5.3.5.5 5 1/2 DIGIT MODE CALIBRATION.

a. Connect the DMM to the Input Standard as specified for the first calibration point in Table 5.12. Set the K-V Divider to .009999X. Apply 0.00000 VDC to the DMM by shorting the input of the K-V Divider.

b. Depress and hold the Calibration Switch.

c. If the reading is not zero (4 digits p-p noise allowed), proceed to step (d); if equal to zero, release the Calibration Switch and proceed to step (f).

d. Increment or decrement the reading with the STORE/DOWN or RECALL/UP keys or GPIB command until the reading is zero.

e. Release the Calibration Switch.

f. Connect the DMM to the Input Standard as specified for the next calibration point in Table 5.12.

g. If the DMM reading is not equal to the Input Standard, proceed to step (h); if equal to the Standard, release the Calibration Switch and proceed to step (k.).

h. Depress and hold the Calibration Switch.

i. Increment or decrement the reading with the STORE/DOWN or RECALL/UP keys (or GPIB Command) until the reading is equal to the Input Standard.

j. Release the Calibration Switch.

k. Repeat steps (f.) thru (j.) for each calibration point in Table 5.12, except the 4 1/2 Digit Mode Scale Factor. At that step, see 5.3.5.5. Calibration is completed.

5.3.5.6 4 1/2 DIGIT MODE SCALE FACTOR CALIBRATION.

a. Switch to the 4 1/2 Digit Mode (depress RESOL Key) and Auto-ranging (depress AUTO Key - verify that AUTO annunciator is ON).

b. Apply +2.0000 VDC and note reading.

c. Apply −2.0000 VDC and note reading.

d. Depress and hold the Calibration Switch.

e. If the opposite polarity readings in (b) and (c) above are equal in magnitude, but not equal to 2.0000, increment or decrement either polarity reading with the STORE/DOWN or RECALL/UP Keys (or GPIB Command) until the readings are 2.0000 + 1 digit.

f. If the opposite polarity readings are not equal in magnitude, increment or decrement either polarity reading until the readings are within ±3 digits of 2.0000.

g. Release Calibration Switch.

5.3.5.7 AVERAGING AC FREQUENCY RESPONSE CALIBRATION–MODEL 5005

5.3.5.7.1 Perform the following instructions when frequency response calibration is required;

a) Connect the AC source to the DMM input terminals

b) Apply the inputs listed in the chart below.

c) Adjust the trimmers listed under "adjust" for the readout indicated. The trimmer locations are shown in Figure 5.5.

Range	INPUT		Adjust	Readout
	AC Voltage	Freq		
1000	250V	80kHz	C2	250.00
1	1V	100kHz	C26	1.00000
10	10V	100kHz	C29	10.0000
100	100V	100kHz	C34	100.000

5.3.5.8 RMS AC FREQUENCE RESPONSE CALIBRATION MODEL 5006

5.2.5.8.1 Perform the following instructions when frequency response calibration is required:

a) Connect the AC source to the DMM input terminals.

b) Apply the inputs listed in the chart below.

c) Adjust the trimmers listed under "adjust" for the readout indicated. The trimmer locations are shown in Figure 5.7.

Range	INPUT		Adjust	Readout
	AC Voltage	Freq		
1000V	500.00	40 kHz	C27*	500.000
1V	1.0000	50 kHz	C9*	1.00000
10V	10.000	50 kHz	C7*	10.0000
100V	100.00	50 kHz	C4*	100.000

*Use an insulated screwdriver when adjusting the capacitors. High voltage present on C27.

5.3.6 Adjustments After Repairs.

5.3.6.1 If major repairs are performed on the Isolator, AC Converter or Ohms Amplifier, offset and bias adjustments associated with these circuits may need adjustment. Also, if repair work is performed in the vicinity of the non-volatile memory, or battery power is interrupted, the contents of

the non-volatile memory may be invalidated. This is indicated by the presence of the message "Error 4" shortly after power-up.

5.3.6.2 ISOLATOR ADJUSTMENT.

a. Input Bias Current Null (R53) - See paragraph 5.3.5.2.

5.3.6.3 INITIALIZING NON-VOLATILE MEMORY.

a. Refer to Table 5.13 for the Function, Range and Input for each Non-Volatile memory calibration point.

Table 5.13 - Inputs for Initializing Non-Volatile Memory

Function	Range	Input Standard (Note 1)
DC	.1V	0.0 VDC
	.1V	+0.1 VDC
	.1V	+0.1 VDC (Note 2)
	.1V	−0.1 VDC
	1V	+1.0 VDC
	1V	−1.0 VDC
	10V	+10 VDC
	10V	−10 VDC
	100V	+100 VDC
	100V	−100 VDC
	1KV	+1000 VDC
	1KV	−1000 VDC
AC	1V	0.0V RMS
	1V	1V RMS, 400 Hz
	10V	10V RMS, 400 Hz
	100V	100V RMS, 400 Hz
	1KV	1000V RMS, 400 Hz
KΩ	100KΩ	0.0Ω (Note 3)
	.1KΩ	100Ω
	1KΩ	1KΩ
	10KΩ	10KΩ
	100KΩ	100KΩ
	1000KΩ	1MΩ
	10,000KΩ	10MΩ

Note 1 - Unless otherwise noted, ± 10% accuracy is adequate.
Note 2 - Select 4 1/2 Digit mode (RESOL Key) and auto-ranging (AUTO Key) for this calibration only. Return to 5 1/2 Digit mode (RESOL Key), fixed range before continuing to the next step.
Note 3 - Either 2-wire or 4-wire connections are satisfactory.

b. At each point in the Table, set the DMM to the indicated Function and Range, and apply the specified input.

c. Depress and hold the Calibration switch.

d. While the Calibration Switch is held depressed, press and release the RESET/NOMINAL Key.

e. Release the Calibration Switch.

5.4 TROUBLESHOOTING.

5.4.1 General.

5.4.1.1 To troubleshoot the DMM and track-down malfunctions it is necessary to be familar with its normal operation. This manual is an important service tool, hence reading the complete manual is recommended.

5.4.1.2 A complete set of schematics for the DMM is contained in Section 6, which includes the parts list and parts lay-out. The components, IC's and logic symbols used in the schematic diagrams are identical to those found in most manufacturers data sheets. Whenever a designator appears which is unique to Racal-Dana, the description follows immediately.

5.4.1.3 The drawing interconnects and continuations to other sheets are indicated in the following manner:

a. Plugs and Jacks: "P" indicates the plug or movable section of the connector and J the jack or stationary connector. P or J with the numbers from 1 to 99 are used on the main PCB or motherboard locations, whereas P or J 100 series are on the front panel location and P or J 200 series represents the rear panel location. The E terminals are used for direct connection to the main PC board.

b. The drawing or schematic connection from one sheet to the next utilize the road-map grid system, with numbers along the horizontal edge and letters along the vertical edge of the drawing. A line terminating with a connection reference of 2B4 would read: sheet two, row B and column 4.

5.4.1.4 The specific types of equipment in the Suggested Equipment column are acceptable for service and provided as a guide in selecting suitable equipment; instruments having operating characteristics equal to or better than those indicated may be substituted. Refer to Table 5.1

Table 5.14 - Test Equipment

ITEM	MINIMUM USE SPECIFICATION	EQUIPMENT
DC Power Supply	Adjustable 0-20 VDS	-
Oscilloscope	100 MHz Band Width	TEK-465
DMM	0.1% DCV	Racal-Dana 4000
Counter	.1 Hz Resolution 10 MHz Ext. Reference Input	Racal-Dana 9000
Logic Clip		Best Source
Logic Probe		Best Source
Logic Comparator		Best Source
Logic Pulser		Best Source
Logic State Analyzer		Best Source
Simulator		Best Source
Emulator		Best Source
Controller	Or Equivalent	HP 9825

5.4.2 Software Troubleshooting.

5.4.2.1 Software and hardware problems may create the same symptoms but the cause may not be related. To isolate this problem, a list of General and Remote Error messages is supplied in Table 5.15. The general error messages numbered 0 to 9 apply to local and remote operations. The messages numbered 10 to 13 apply to GPIB operation only.

Table 5.15 - General and Remote Error Messages

Error Message No.	Error Message
	GENERAL ERROR MESSAGES
1	Not in the DC function, 0.1 range when executing DIGITAL ZERO command.
2	Attempting to execute DIGITAL ZERO command with an input voltage applied or the input open-circuited. Connect a short across input terminals and repeat DIGITAL ZERO command.
3	The microprocessor's on-board RAM is defective (U35 on the motherboard).
4	The contents of the non-volatile memory have been disrupted, therefore the instruments calibration should be verified.
5	A digitizer offset greater than 1000 digits was measured during execution of DIGITAL ZERO command
6	Percent Deviation of $\geq 10^{10}$% while in the Percent Function.
7	The RAM is defective, U22 and/or U31 on the motherboard.
8	An attempt was made to store a overload reading to a register inside the DMM or an attempt was made to store > 99.5959 hours into a Time function register.
9	An attempt was made to recall a program setting from the program buffer before setting was stored to the program buffer.
	GPIB ERROR MESSAGES
10	Recall of a constant whose value is empty set, for example - sending an "L7" command to a DMM will cause this error if the LOW, AVERAGE, and HIGH constants are the empty set (no readings taken yet.)
11	Triggered too fast or too often.
12	Syntax error during GPIB programming.
13	Option not installed.

5.4.3 Hardware Troubleshooting.

5.4.3.1 To service hardware, it is important to know the normal operation of the DMM. The block diagram in Figure 5.5 is presented as an overview to aid familiarization of the electrical configuration and Figure 5.4 indicates the test point on the parts layout of the mainframe PCB assembly. The schematic drawings in Section 6 complete the necessary details required to troubleshoot the DMM.

5.4.3.2 The DC voltages distributed throughout the DMM are a reliable status indicator and any deviation from normal can be readily observed. Typical operating voltages are supplied in Table 5.15 for the major circuits on the PCB. The left column names the circuits and the instructions are listed across the top. The chart information progresses from left to right. Using the circuit listing 'DIGITAL SUPPLY' for example, it reads:

a. Required voltage column reads +5VA and +5VB.

b. Parts Lay-out Reference Column: A guide to test-point locations.

c. Meter Probe column specifies the test-point connection. It reads Positive TP13 and Negative common TP5.

Table 5.16 - Power Supply Voltage Checks (Page 6-5)

Tests → / Circuit ↓	Required Voltage DC ±10%	Parts Layout Ref.	Meter Probes Pos. Neg.	Reading OK	Move Probe To →	Move Probe To →	Move Probe To →	AC Reading
Digital Supply	+5VA	Fig. 5.8	Pos. TP13 Neg. TP5	No Next →	U50-IN No →	CR14, Cath. No →	→	Term 7 & 9 Power Trans.
	+5VB	Fig. 5.8	Pos. TP14 Neg. TP5	No Next →	U51-IN No →	CR15, Cath. No →	→	Term 7 & 9 Power Trans.
Non-Voltile Memory	+9V Un-Reg.	Fig. 5.8	Pos. CR14C Neg. TP5	No Next →	(Note: When +5VA or B OK, Then +9V OK) →			Term 7 & 9 Power Trans.
Analog	(+30V)	Fig. 5.8	Pos. CR22 Neg. TP12	No Next →	CR22, Cathode (+30V) No →	Lower Side R81 (+36V) No →	CR20+ (+36V) No →	Term 10 & 16 Power Trans.
Analog	(−30V)	Fig. 5.8	Pos. CR25 Neg. TP12	No Next →	CR25, Anode (−30V) No →	Left Side of R82 (−36V) No →	CR20− (−36V) No →	Term 10 & 16 Power Trans.
Isolator	+36V Un-Reg.	Fig. 5.8	Pos. CR20+ Neg. TP12	No Next →	(Note: When +30V OK, Then +36V OK) →			Term 10 & 16 Power Trans.
	−36V Un-Reg.	Fig. 5.8	Pos. CR20− Neg. TP12	No Next →	(Note: When −30V OK, Then −36V OK) →			Term 10 & 16 Power Trans.
AC-DC Ohms	+12V Un-Reg.	Fig. 5.8	Pos. U19 Pin 16 Neg. TP12	No Next →	U48-IN No →	CR-16+ No →	→	Term 11 & 15 Power Trans.
Op-Amps	−15V	Fig. 5.8	Pos. Can AR6 Neg. TP12	No Next →	No → U49-IN	No → CR16−	→	Term 11 & 15 Power Trans
Relay Drive	+12V Un-Reg.	Fig. 5.8	Pos. CR18-Cath. Neg. TP12	No Next →	No →	No →	No →	Term 12 - 14 Power Trans.
A-D Converter	+8V	Fig. 5.8	Pos. U33 Pin 16 Neg. TP12	No Next →	U52-IN No →	→	→	Term 12 - 14 Power Trans.
Non-Vol Memory Battery	+3V	Fig. 5.8	Pos. BT1-Pos. Neg. TP12	No Replace				
DC Supply	+5V	Fig. 5.8	Pos. CR21-Pos. Neg. TP12	No Next →	Pos. CR14 Cath. +9V. No →	→	→	Terminals 7 & 9 Power Transformer

5.4.3.3 When a voltage problem develops, (which usually alters the performance of the DMM, the mean-time-between failures (MTBF) indicates that capacitor failure can most often be the cause for the failure (filter or bypass). Therefore, whenever the DC voltages are below normal, the capacitors in that circuit should be examined as a possible fault source. For catastrophic power supply failures (smoke is evident), place a current limiter in series with the AC line. A lamp with half the unit rated wattage, in series with the line, will limit the current drain to a safe value, permitting service to be conducted.

5.4.3.4 Voltage problems are most often caused by temperature-related component failure, usually accompanied by an increased current drain and excessively high temperature at the specific component. Tracing the symptom can be simplified with conventional bench equipment listed next:

a) AC inline ammeter (mid-scale should read average current drain.)

b) Temperature probe (Racal-Dana T10).

c) Can of Cool-it or Freeze-it spray coolant. When a voltage problem develops, the voltage drop follows an increased current drain and excessive temperature increase at the faulty component. Spray the suspected component with cool-it and note the voltmeter and ammeter readings.

5.4.3.5 Digital debugging or troubleshooting procedures require additional test equipment compared to conventional electronic service. The digital test equipment listed in Table 5.1 is representative of the equipment available for digital and microprocessor service, although preference remains with the individual technician. Only a brief description of each unit is presented for the technical center needing digital equipment:

a) LOGIC CLIP: Instantly displays the logic states of all DIP pins (TTL or DTL). The LED's follow the logic state changes (level changes).

b) LOGIC PROBE: Permits examination of one pin, indicating if the state is high or low. The probe blinks to indicate the presence of a pulse train.

c) LOGIC COMPARATOR: Clips on to a powered TTL chip and displays any logic state difference between the IC under test and a reference IC. Logic differences are identified to a specific pin.

d) LOGIC PULSER: This probe injects a narrow pulse into the circuit to determine if a gate is working. The gate will switch state.

e) LOGIC STATE ANALYSER: A CRT display device that can exhibit up to 32 channels of digital input. The data words in process can be examined in relation to time and events.

f) SIMULATOR: This system employs software to replace the hardware functions. The software program will generate the same outputs as the hardware device.

g) EMULATOR: The emulator executes the processor programs in real time by connecting the emulator DIP connector into the MPU socket and inserting the MPU into the emulator probe. This device is usually a service feature of the Chip manufacturer.

5.4.3.6 Troubleshooting practices basically require the individual's logical deductions to solve product failure. The cases presented in Troubleshooting Table 5.17 list the causes of the problem, the probably cause generating the symptoms and Suggested Corrections. The test equipment employed is left to the individual's preference.

LEGEND

1. POWER SUPPLY
2. DC,AC,3-POLE FILTER
2A. AC CONVERTER
3. OHMS
4. RELAY DRIVE
5. A/D CONVERTER
6. μP CONTROL & NON-VOL
7. OCI-1,2,3
8. GPIB
9. LED DISPLAY

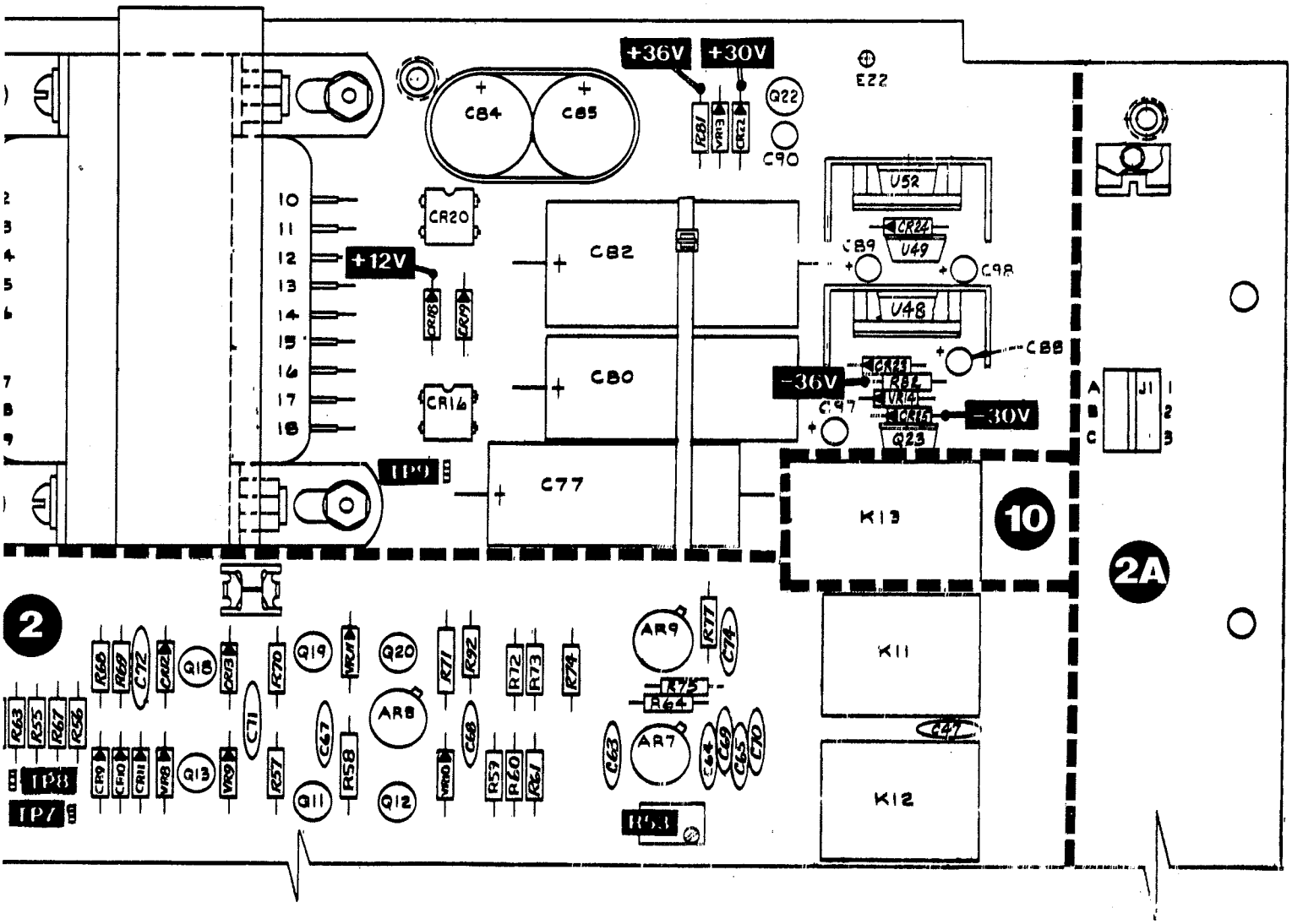
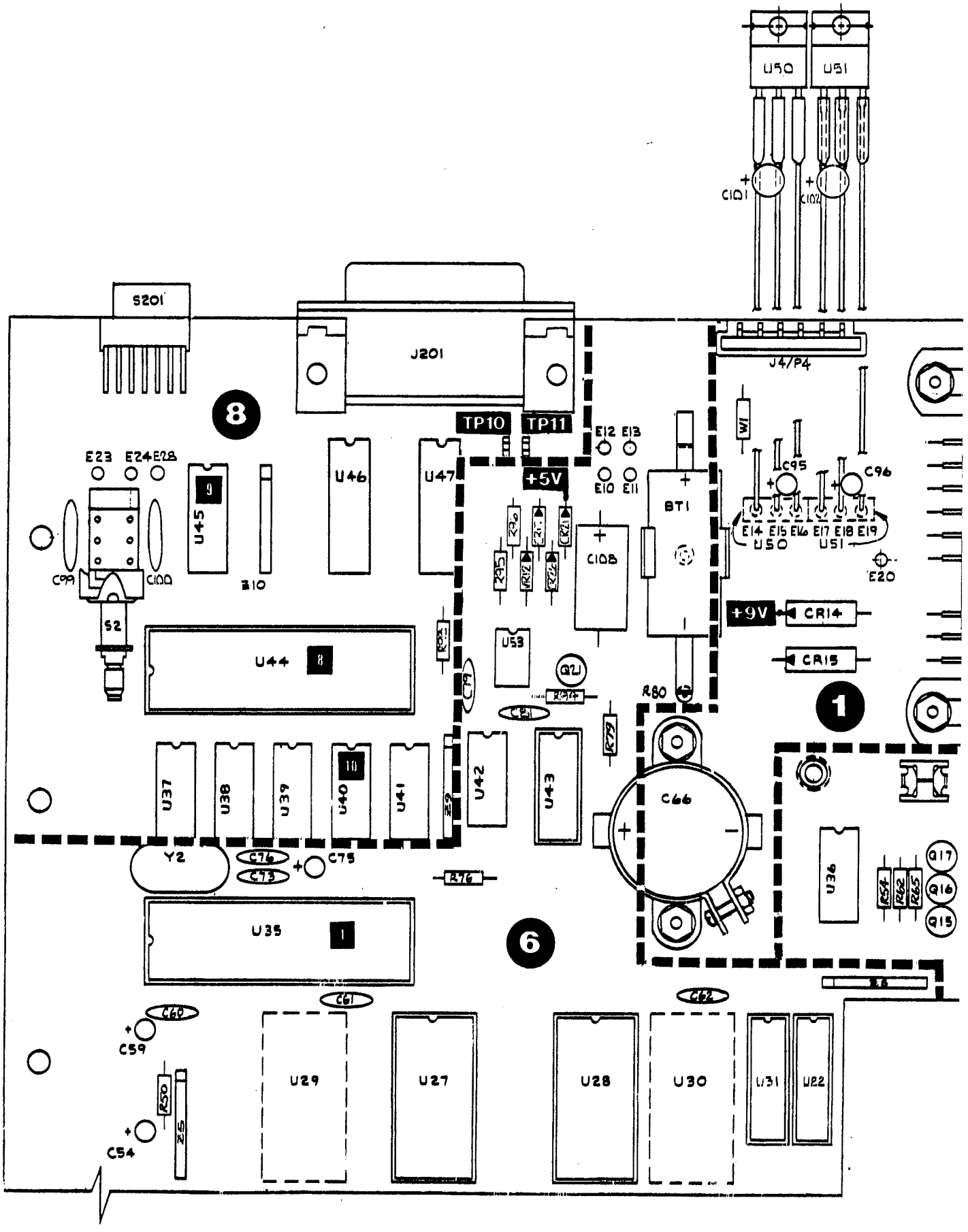


Figure 5.8 - Test Point Location


U50
U51
C101
C102
S201
J201
J4/P4
8
TP10
TP11
E12 E13
E10 E11
+5V
E23 E24 E28
U45
U46
U47
BT1
C95
C96
E14 E15 E16 E17 E18 E19
U50
U51
E20
C99
C100
E10
C108
+9V
CR14
CR15
S2
U44
U53
Q2J
R80
1
U37
U38
U39
U40
U41
U42
U43
C66
Y2
C76
C73
C75
R76
U36
Q17
Q16
Q15
U35
6
C61
C62
C60
C59
C54
U29
U27
U28
U30
U31
U22

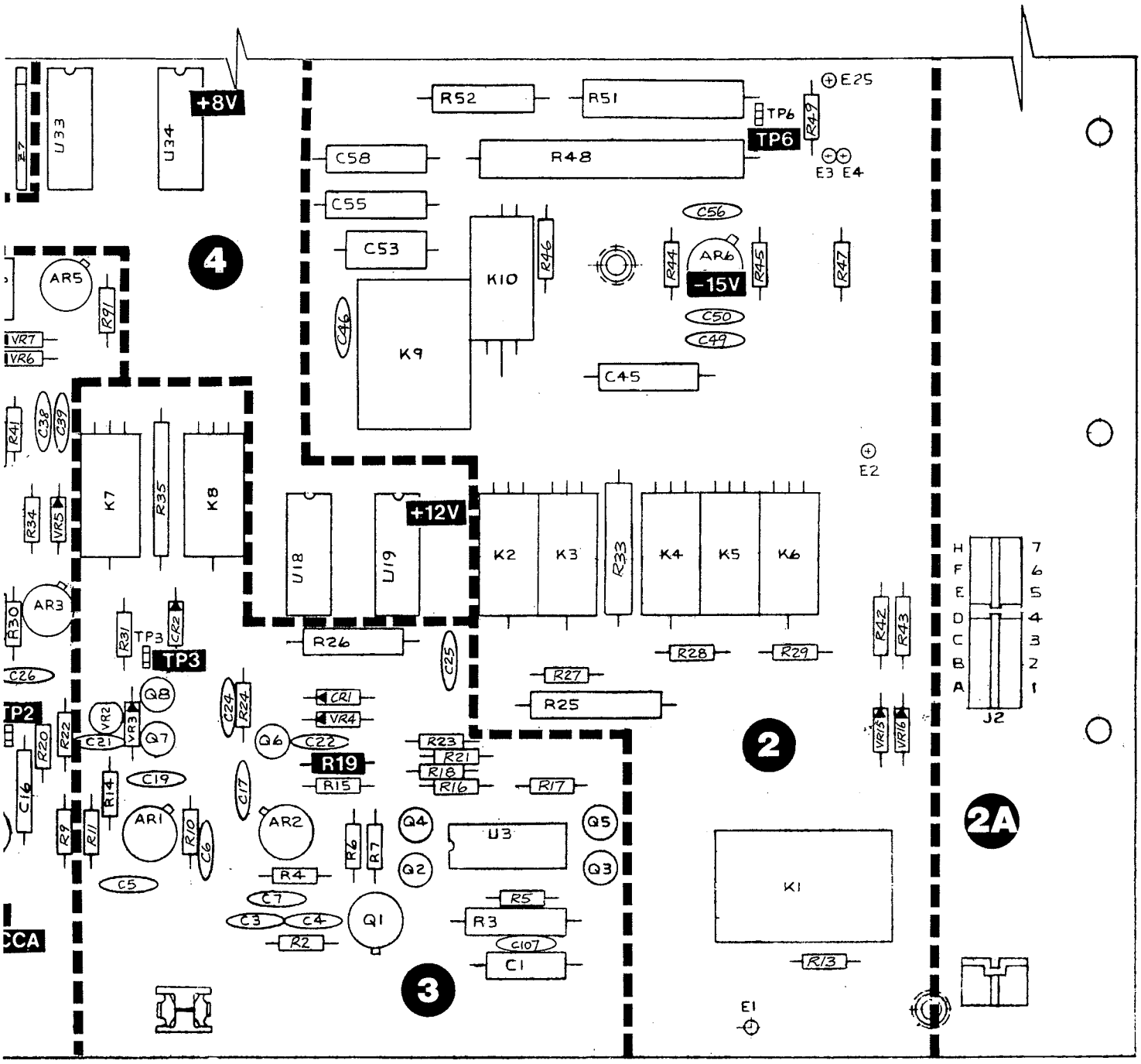


Figure 5.8 - Test Point Location continued

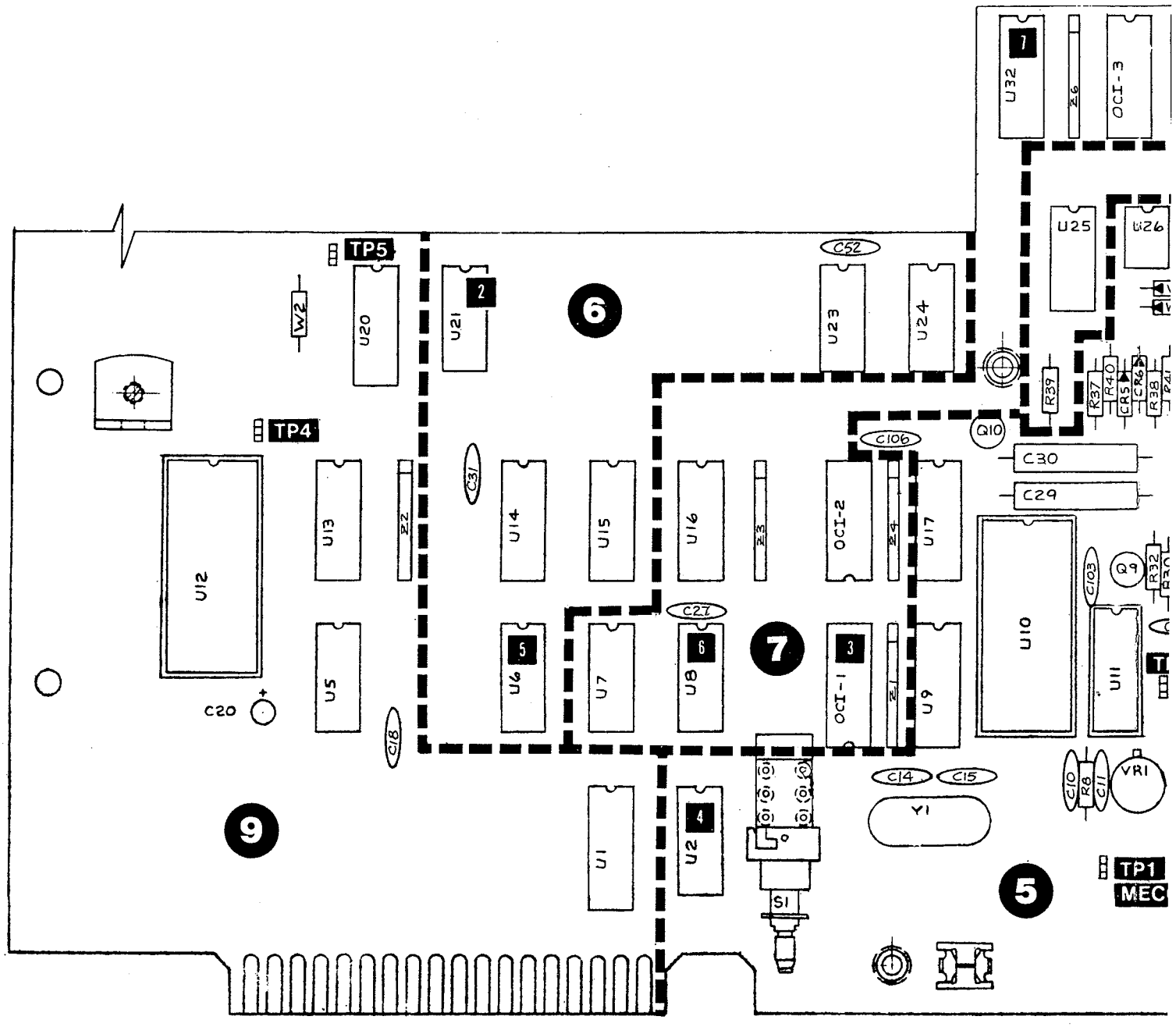

TP5
TP4
W2
U20
U21
2
6
U32
Z6
OCI-3
U25
U26
C52
U23
U24
R39
R37
R40
CR5
CR6
R38
R41
Q10
C106
C30
C29
U12
U13
Z2
C31
U14
U15
U16
Z3
OCI-2
Z4
U17
U10
C103
Q9
R32
U11
C27
5
U6
U7
6
U8
7
3
OCI-1
Z1
U9
C20
C18
C14
C15
Y1
C10
R8
C11
VR1
9
U1
4
U2
S1
5
TP1
MEC

Table 5.17 - Troubleshooting Examples

SYMPTOMS	PROBABLE CAUSE	SUGGESTED CORRECTIONS
EXAMPLE–A DMM displays "5004" during power-up DMM displays "5003" during power-up	 U20 data buffer may be defective. U28 ROM may be defective.	 Replace U20 Replace U28
EXAMPLE–B DMM displays model number and/or error message, then fails to proceed. (Hangs-up).	 μP unable to control inguard or outguard logic; or μP unable to read from logic using 74LS367 buffers.	 Scope address decoder outputs U14 pins 15, 14, 13, 12, 11, 10 and 9 or U15 pins 14 and 13. Watch for narrow, negative-going pulses which indicate that the μP is continually waiting for some hardware events or is trying unsuccessfully to initiate a hardware event. The affected address decoder output gives an indication of the hardware involved.
EXAMPLE–C DMM continues to take readings when in "SINGLE" or "RECALL" mode.	 μP receiving NMI (non-maskable interrupt) on U35-6 OR loss of "read control" signal somewhere between μP and A/D converter	 Verify operation of U2 interrupt and associated circuitry Check read control signal as it propagates from U35-15 μP chip through OCI-3 to U10-26 digital control chip.
EXAMPLE–D Function LED's correspond to selected function but relays don't always change state to match newly selected function.	Defective Dc power supply in Analog Section Register Load Hardware (U33-U34) defective.	Verify power supplies and replace components as necessary. Alternately press front panel DC and AC keys rapidly and verify the output waveforms from OCI-3 all pins. The signal will swing between 1-1/2 V and 6-1/2 V minimum. They should track the driving waveforms which are partially shown in Table 5.16 Performance tests. Also, verify the operation of U32, U33 and U34. Verify the presence of strobe pulse on U33/U34-1 after last clock pulse on U33/U34-3

Table 5.17 - Troubleshooting Examples continued

SYMPTOMS	PROBABLE CAUSE	SUGGESTED CORRECTIONS
EXAMPLE–E DMM ignores keyboard.	Key on keyboard is already "pressed" (shorted) OR μP unable to read keyboard status from keyboard three-state buffer. OR Defective GPIB hardware causes DMM to go to "remote" at power-up	Troubleshoot keyboard rows and columns switch operation Verify the operation of U13-keyboard buffer. Verify that "remote" LED is not lit after completion of power-up sequence. If LED is lit, replace U44, GPIA.
EXAMPLE–F "ERROR 5" displayed during digital zero command	U26 - M/Z switch failing to switch AR5-3 to zero volts during digital zero. OR A/D converter IC's are suspect OR A/D output signals lost as they propagate through U17-U9 digitizer drives, OCI-1/2 op-to couplers, and U16 data driver.	Verify a logical '1' on U26-2 during digital zero. If not present, see suggested corrections for Example–D, otherwise verify other analog and digital signals on U26. Replace U10 and/or U11. Troubleshoot chips, checking for "stuck" levels at each stage.

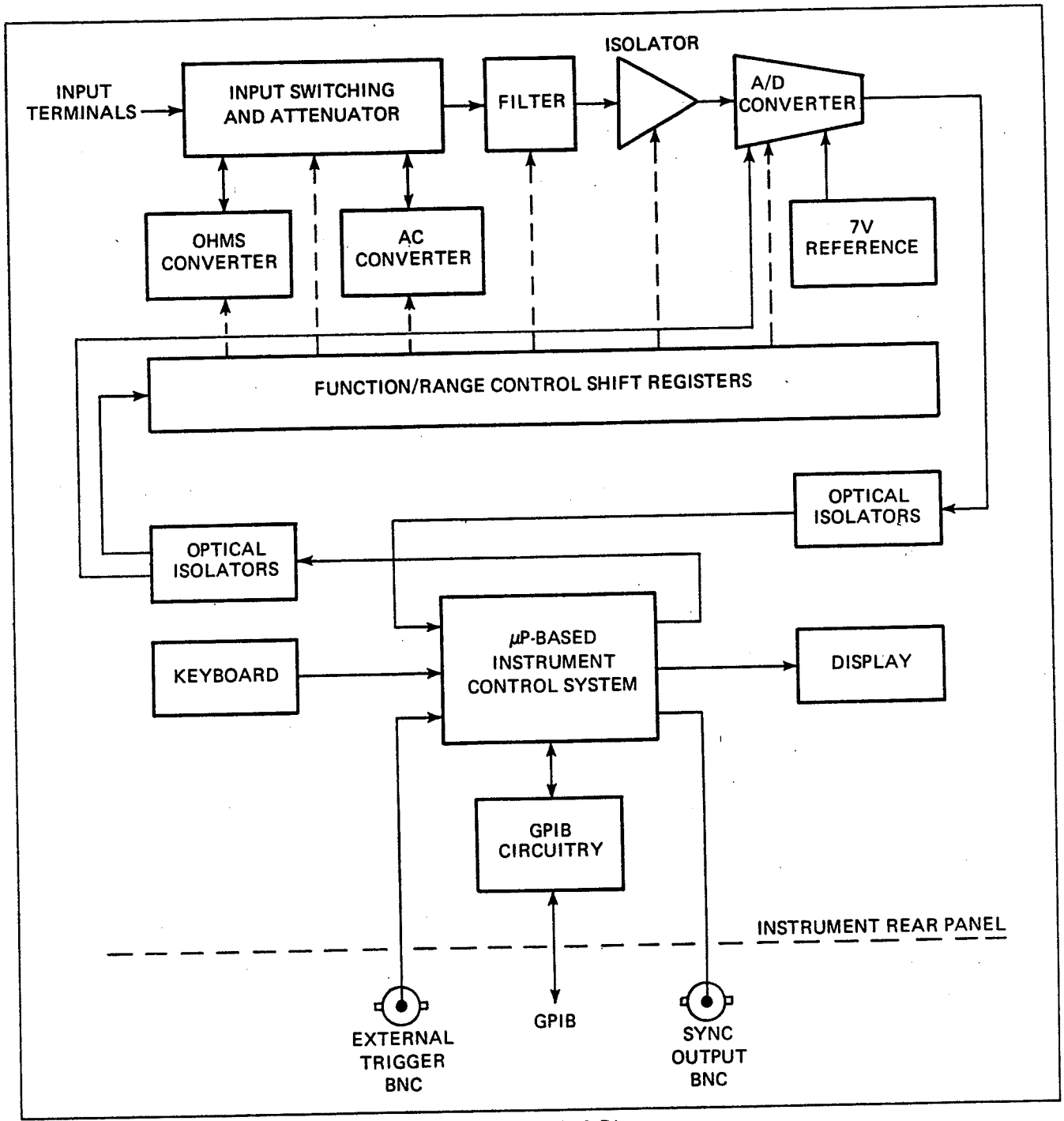


Figure 5.9 - DMM Block Diagram

5.4.4 Troubleshooting Performance Tests.

5.4.4.1 The performance tests are designed to isolate a malfunction to a replaceable module or printed circuit board. In some cases where the printed circuit board is large and complex, the test is designed to isolate the malfunction to a functional area of the board.

5.4.4.2 Both the unit and subassembly performance tests present setup instructions, step by step for monitoring the circuit under test, and performance standards listed as voltage levels or oscilloscope waveforms. Parts layout drawings are provided to aid in locating the test points on the assembly board.

5.4.4.3 Test points called out in the performance tests may be actual physical test points provided as convenient test points or they may simply be circuit locations such as the end of a resistor or the emitter of a transistor. In either case the test points appear in the performance test tables as black squares.

5.4.4.4 Note that the test points are numbered sequentially from the start of the performance tests and progress to the end. The performance standard for each test point is shown in the table if it is a voltage standard; the waveform standards are provided on waveform illustration pages immediately following the performance test table. The numbered test points refer to square black test point flags 1 appearing on the assembly drawing in the Drawing Section (6).

5.4.4.5 To perform subassembly performance tests refer to the appropriate test table, perform the preliminary test setup presented as the first few steps of the test. When the setup is complete proceed with test and verify that the measurement at each test point is within tolerances called for in the performance standard column of the test. If at any point in the test you do not obtain the required voltage or signal refer to the appropriate schematic to determine the area of the malfunction. Resort to conventional troubleshooting methods to identify the faulty component or circuit. The term conventional troubleshooting methods as used here means checking individual semiconductors, resistors and capacitors in and around the area of malfunction.

WARNING

These servicing instructions are for use by qualified personnel only. To avoid electric shock, do not perform any servicing other than that contained in the instructions unless you are qualified to do so.

5.4.4.6 Tables 5.18 through 5.20 present the unit performance tests. Note that the tables contain performance standards for voltage measurements and waveforms. The tolerance required for troubleshooting is looser than operating tolerances because the technician is generally looking for the presence of the signal rather than an exact high tolerance standard. This allows the use of a much broader range of test equipment and also allows the use of test equipment that is not subject to high accuracy calibration requirements.

5.4.5 Battery Replacement For Non-Vol Circuit.

5.4.5.1 During power-down periods when the DMM is not AC line powered, a Lithium battery (BT1 located in section 1) maintains the required voltage to the Non-Volatile memory circuit, which includes the CMOS RAM U43. When the voltage drops below 2.3V, the RAM will lose its CAL constants. This causes the "ERROR 4" message to be displayed next time the DMM is powered-up.

5.4.5.2 It is important to recognize that the displayed error message indicates that the contents of the Non-Vol memory were disrupted and most often indicates a discharged battery. If the battery voltage to U43-16 with power-down exceeds 2.3V, other components in the circuit may be at fault.

5.4.5.3 STEPS TO REPLACE BT1 BATTERY.

a) Apply power to the DMM. Verify that it completes the power-up sequence listed in paragraph 3.2.2.

WARNING

During removal of the bottom guard-shield plate, care must be taken that the non-volatile memory battery supply (BT-1) is not short-circuited, losing all CAL constants stored in memory. When the guard-shield is freed, lift directly away from or at right-angle (orthogonal) to the PCB. Do not slide the shield over the PCB.

b) CAUTION: The DMM is still powered-up. Use a battery powered or un-grounded soldering iron to unsolder the battery tabs from the motherboard and remove the old battery.

c) Observe polarity and install the new battery in the same position.

WARNING

Lithium batteries may explode if short-circuited, recharged, disassembled, heated, disposed of in fire, or exposed to temperatures above 90°C. Battery leakage may forewarn a problem.

5.4.5.4 Preventative Maintenance: Use the following procedure to check the battery condition:

a) Turn-off the AC power to the DMM.

b) Wait 30 seconds.

c) Measure the voltage drop with a one millivolt resolution DVM across R80, the 1 Kohm resistor in series with the battery.

d) The voltage drop across R80 should be less than 20 mV (battery drain 20 μA).

5.4.5.5 Suggested Battery Replacement Interval can be determined from Figure 5.10. It is supplied as an aid to determine how often the Lithium battery, BT1, should be replaced. Notice that the worst-case battery drain occurs if the instrument is stored at high temperatures with the power off (3 year replacement interval). For most applications, a 4 year replacement interval is suggested.

5.4.6 Lithum Battery Safety Precautions

5.4.6.1 Do not store the batteries in areas where the ambient temperature exceeds 90^{o} centigrade.

5.4.6.2 Verify that the discarded battery is completely discharged. Connecting a 10 ohm one-watt resistor across the terminals for 24 hours will completely discharge the battery.

5.4.6.3 Return the completely discharged battery to your local Racal-Dana Representative, service depot or locally assigned disposal areas.

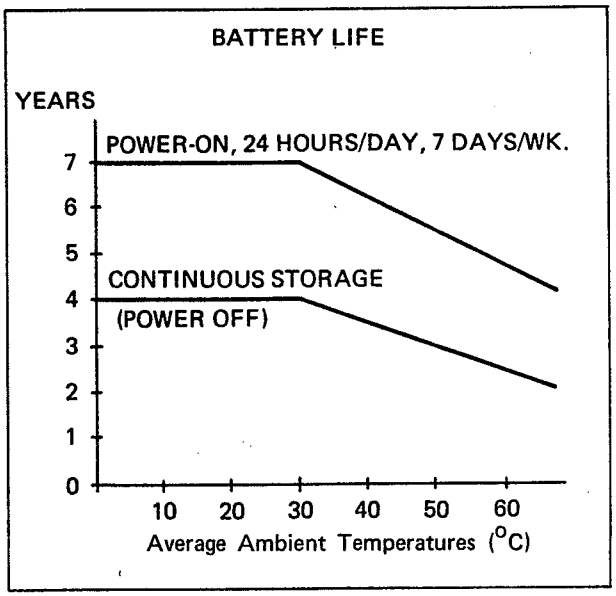


Figure 5.10 - Battery Life Graph

Table 5.18 - **Digital Section Performance Test**

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Using conventional techniques, the Digital Section can only be tested to the point where certain "Knowns" can be verified. If the proper waveforms are not observed, the nearest Racal-Dana serivce center should be contacted.					
All measurements in this table are referenced to TP4, Digital Common. Power Switch: ON				Test Points Shown on Figure 5.4	
Disconnect any cables connected to Rear Panel GPIB and BNC Connectors	+5 VA +5 VA +5 VB $\overline{\text{Reset}}$ $\overline{\text{NMI}}$	U35 Pin 40 U35 Pin 6	1 1		+5V ± .25 VDC +5V ± .25 VDC +5V ± .25 V +2.5V to +5.25V with no excursions below +2.5V
Set Scope Trigger To Internal, Channel 1, + Slope	μP Clock E	U21 Pin 11	2		Waveforms #7, Ch. 1
	Inverse Signal $\overline{\text{E}}$	U21 Pin 10	2		Waveforms #7, Ch. 2
	Address Bus	U35 Pins 9 to 20 and 22 to 25	1		See Note Below
	Data Bus	U35 Pins 26 to 33	1		See Note Below
	VMA	U35 Pin 5	1		See Note Below
	R/$\overline{\text{W}}$	U35 Pin 34	1		See Note Below
	W/$\overline{\text{R}}$	U21 Pin 8	2		See Note Below
Scope Trigger Set To: Internal, + Slope, Channel 1	Digit Strobe Sync D6 (After Opto-isolation)	OCI1 Pin 11	3		Waveforms #2, Ch. 1
	1 KHz (After Opto-isolation) (approx. .83 KHz in 50 Hz Machine)	OCI1 Pin 14	3		Waveforms #2, Ch. 2

Note: These waveforms are asynchronous TTL signals. If the signals are always high or low at this point, it is an indication of a Fault.

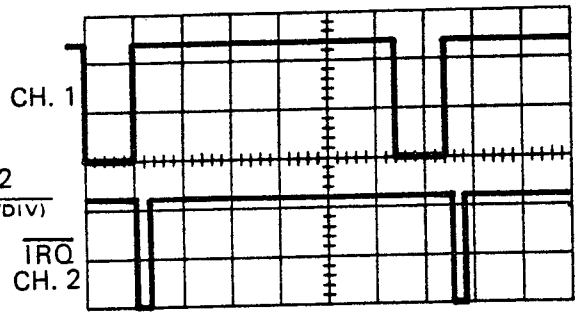
Table 5.18 - **Digital Section Performance Test continued**

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Instrument in "Hold" Mode (Press "SINGLE" Key on Keyboard) Scope Trigger Set To: Internal, – Slope, Channel 1	Clock to Interrupt - Control FF	U2 Pin 11	4		Waveforms #1, Ch. 1
	$\overline{IRQ}$ Input to μP	U35 Pin 4	1		Waveforms #1, Ch. 2
Instrument in "Hold" mode (Press "SINGLE" Key on Keyboard) Scope Trigger Set To: Internal, – Slope, Channel 1	$\overline{DSPE}$	U6 Pin 8	5		Waveforms #5, Ch. 1
DMM Set to Internal Trigger (Press "Track" Key) 4 1/2 Digit Mode (Toggle "RESOL" Key if required) Scope Trigger Set To: Internal, + Slope, Channel 1	$\overline{\text{End of Conversion}}$ (After Opto-isolation and Schmitt Trigger Inversion)	U8 Pin 11	6		Waveforms #4, Ch. 1
	Rdg Rdy (Reading Ready)	U8 Pin 9	6		Waveforms #4, Ch. 2
DMM Set to Internal Trigger (Press "Track" Key) 4 1/2 Digit Mode (Toggle "RESOL" Key if required)	Sync Output	Sync Output BNC (Rear Panel)	Rear Panel BNC		Waveform #3
Scope Trigger Set To: Internal, – Slope, Channel 1 Alternately Press "10" and "100" Range Keys at a Rapid Rate Scope Trigger Set To: Internal, + Slope, Channel 1	CLK	U32 Pin 7	7		Waveforms #6, Ch. 1
	Strobe	U32 Pin 2	7		Waveforms #6, Ch. 2

Table 5.18|- Digital Section Performance Test continued

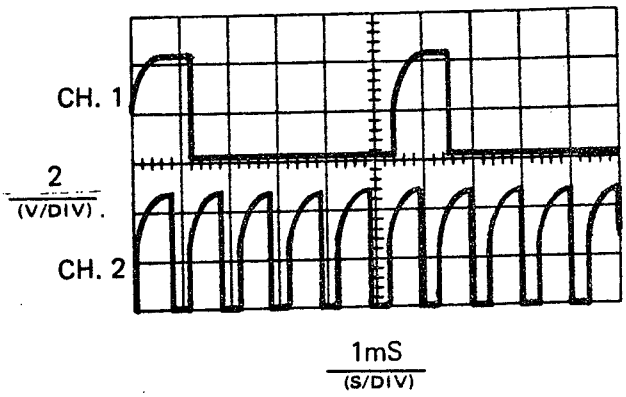
1 (NO.)

SEE NOTE 1



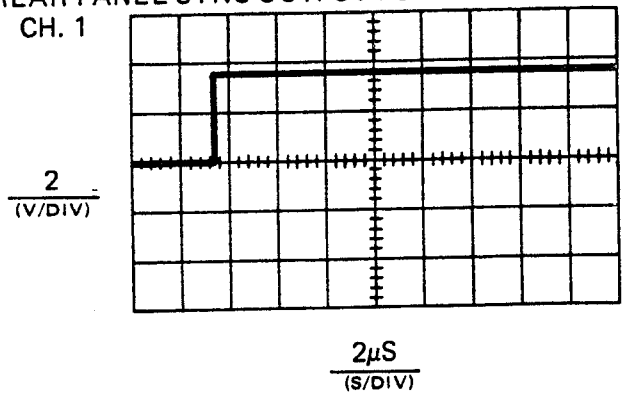
2 (NO.)

SEE NOTE 1



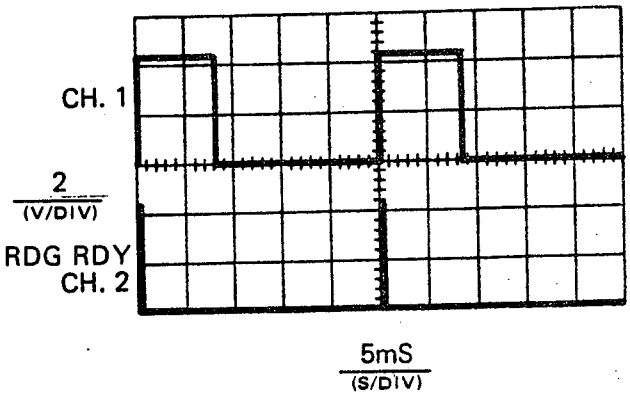
3 (NO.)

REAR PANEL SYNC OUTPUT PULSE

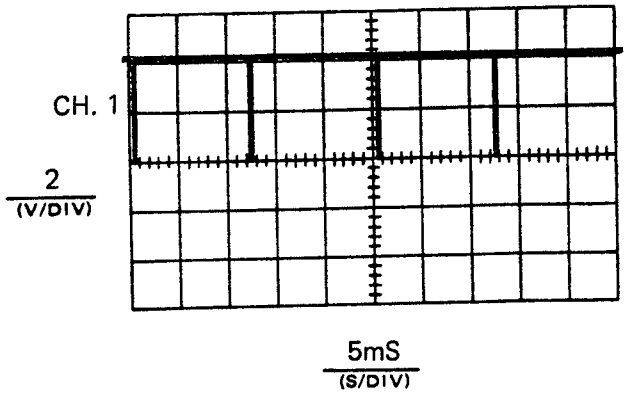


4 (NO.)

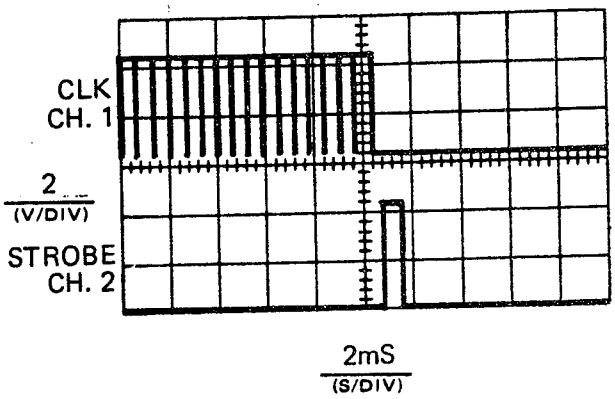
SEE NOTE 1



5 (NO.)



6 (NO.)



NOTE 1 WAVEFORMS ARE SHOWN FOR A 60 Hz UNIT. WAVEFORMS TAKEN FROM A 50 Hz UNIT WILL BE 10% LOWER IN FREQUENCY.

Table 5.18 - Digital Section Performance Test continued